EE 505

Lecture 27

ADC Design

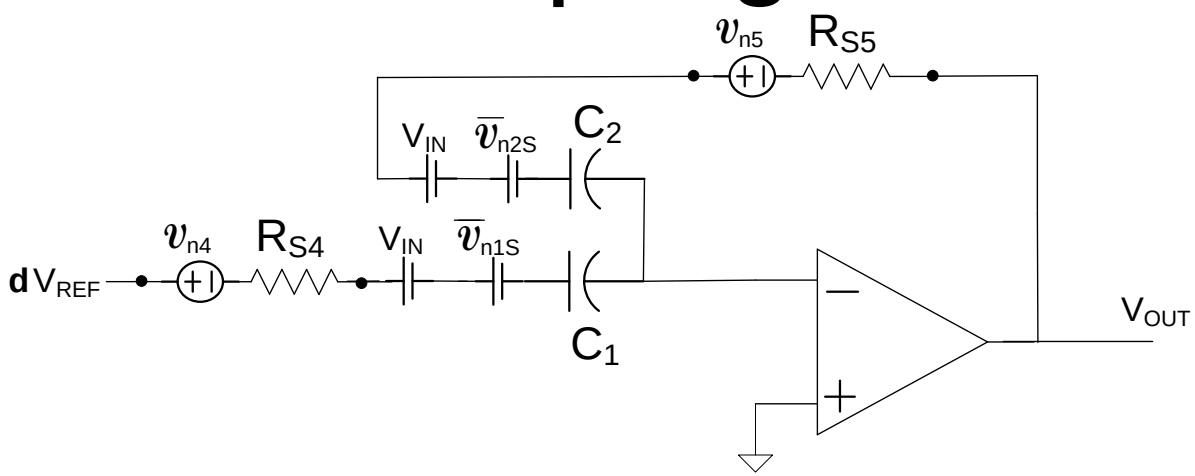
- Pipeline
  - Aperture Uncertainty
  - Cyclic Architectures
  - Eliminating input S/H

SAR ADC Design

Oversampled Data Converters

Review

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

If the ON impedance of the switches is small and it is assumed that $C_1=C_2=C$, $R_{S4}=R_{S5}=R_{SW}$, it can be shown that for $C_1=C_2$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{2C} + \frac{kT}{4} R_{SW} GB}$$

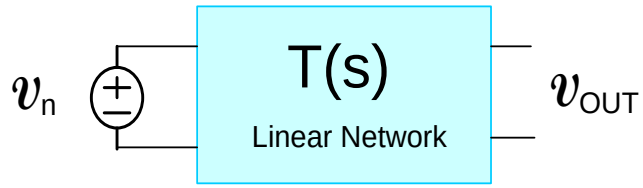
Too much GB or too large of R_{SW} can increase sampled noise voltage

Too small of R_{SW} will not derive any benefit and will increase power, area, and driving problems

GB must be large enough to have complete settling

Review from Last Lecture

Sampling Noise



Theorem 1 If $v_n(t)$ is a continuous-time zero-mean noise source with power spectral density S_V, then the spectral density of v_{OUT} is given by the expression

$$S_{V_{OUT}} = \left|T(s)\right|^2_{s=j\omega} S_V$$

Theorem 2 If $v(t)$ is a continuous-time zero-mean noise voltage with power spectral density S_V, then the RMS value of the continuous-time noise is given by

$$V_{RMS} = \sqrt{\int_{f=0}^{\infty} S_V \, df}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced T seconds apart..

Review from Last Lecture

Sampling Noise

Theorem 3 If V(t) is a continuous-time zero-mean noise voltage and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as

$$V_{RMS} = \hat{V}_{RMS}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced T seconds apart..

Review from Last Lecture

Sampling Noise

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Theorem 4 If V(t) is a continuous-time zero-mean noise source and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …. then the standard deviation of the random variable V(kT), denoted as $\sigma_{\hat{V}}$ satisfies the expression

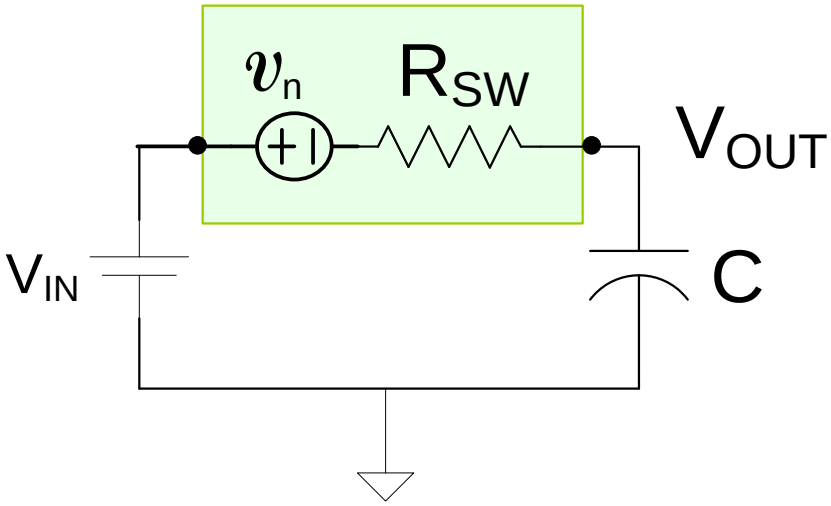
$$\sigma_{\hat{V}} = V_{RMS} = \hat{V}_{RMS}$$

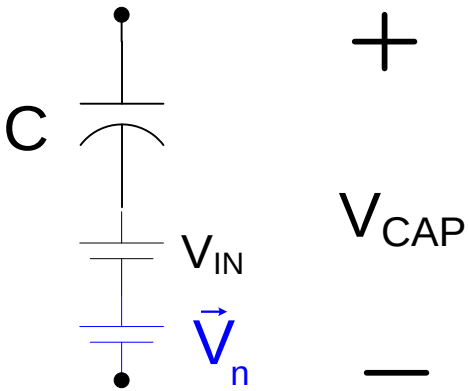
Theorem 5 The RMS value and the standard deviation of the noise voltage that occurs in the basic switched-capacitor sampler is related to the capacitor value by the expression

$$\hat{V}_{RMS} = V_{RMS} = \sigma_{\hat{V}} = \sqrt{\frac{kT}{C}}$$

Review from Last Lecture

Sampling Noise





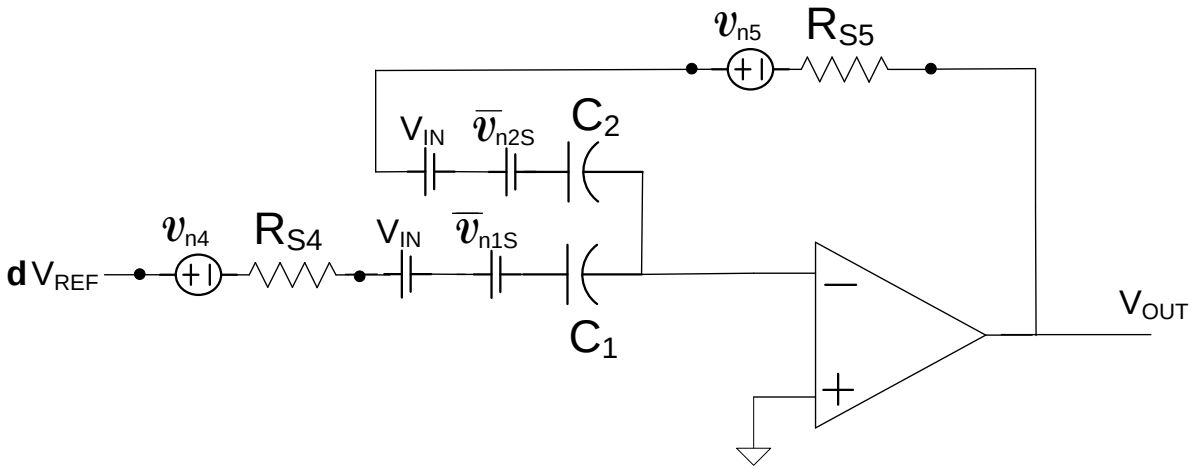
$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

$$\hat{v}_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

Key Result, Continuous-time noise at V_{OUT}

Key Result, Discrete-time noise at V_{OUT}

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

If the ON impedance of the switches is small and it is assumed that $C_1=C_2=C$, $R_{S4}=R_{S5}=R_{SW}$, it can be shown that noise on output is

$$v_{4\text{-}5RMS} = \sqrt{kTR_4GB}$$

$$\hat{v}_{IN\text{-}RMS\phi_2} = \sqrt{\frac{2kT}{C} + kTR_4GB}$$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{2C} + \frac{kTR_4GB}{4}}$$

Review from Last Lecture

Sampling Noise

When is the continuous-time SC noise really of concern?

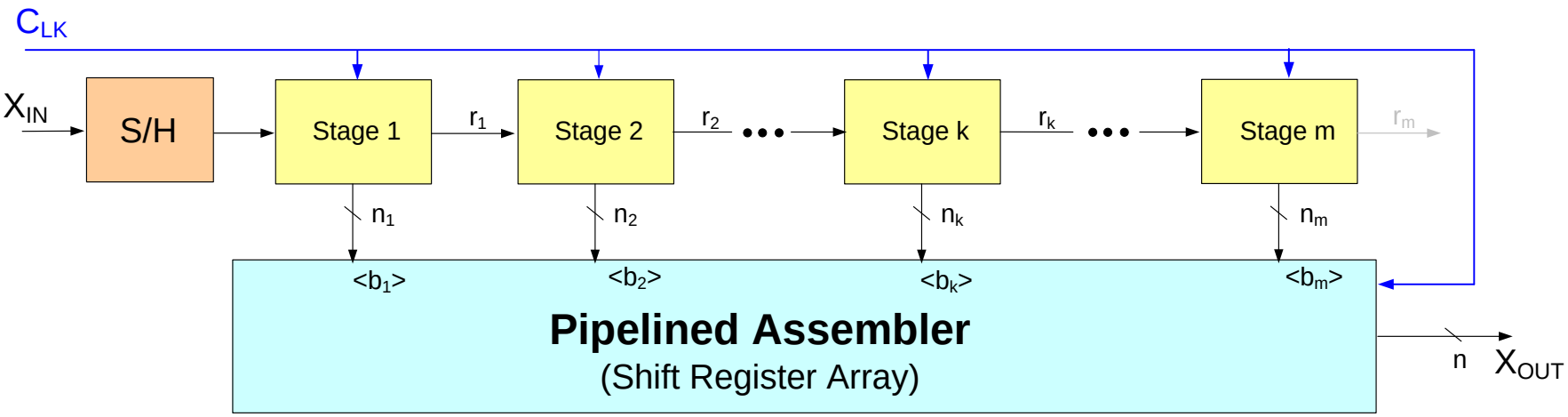
$$R_{MAX} = \frac{1}{kT2^{2n_{ST}+2}\left(n_{ST}+1\right)2\ln 2 f_{CLK}}$$

$R_{MAX}(fCLK,n)$

Clock Speed

Resolution	10	100	1K	10K	100K	1M	10M	100M	1G
4	4.7E+15	4.7E+14	4.7E+13	4.7E+12	4.7E+11	4.7E+10	4.7E+09	4.7E+08	4.7E+07
5	9.8E+14	9.8E+13	9.8E+12	9.8E+11	9.8E+10	9.8E+09	9.8E+08	9.8E+07	9.8E+06
6	2.1E+14	2.1E+13	2.1E+12	2.1E+11	2.1E+10	2.1E+09	2.1E+08	2.1E+07	2.1E+06
7	4.6E+13	4.6E+12	4.6E+11	4.6E+10	4.6E+09	4.6E+08	4.6E+07	4.6E+06	4.6E+05
8	1.0E+13	1.0E+12	1.0E+11	1.0E+10	1.0E+09	1.0E+08	1.0E+07	1.0E+06	1.0E+05
9	2.3E+12	2.3E+11	2.3E+10	2.3E+09	2.3E+08	2.3E+07	2.3E+06	2.3E+05	2.3E+04
10	5.2E+11	5.2E+10	5.2E+09	5.2E+08	5.2E+07	5.2E+06	522353.4	52235.3	5223.5
11	1.2E+11	1.2E+10	1.2E+09	1.2E+08	1.2E+07	1.2E+06	119706	11970.6	1197.1
12	2.8E+10	2.8E+09	2.8E+08	2.8E+07	2.8E+06	2.8E+05	27624.46	2762.4	276.2
13	6.4E+09	6.4E+08	6.4E+07	6412821	641282.1	64128.21	6412.821	641.3	64.1
14	1.5E+09	1.5E+08	1.5E+07	1496325	149632.5	14963.25	1496.3	149.63	14.96
15	3.5E+08	3.5E+07	3.5E+06	350701.2	35070	3507	350.7	35.07	3.51
16	8.3E+07	8.3E+06	8.3E+05	82517.92	8252	825	82.51792	8.25	0.83
17	1.9E+07	1.9E+06	194834	19483.4	1948	195	19.4834	1.94834	0.194834
18	4.6E+06	4.6E+05	46144.89	4614.5	461.4	46.1	4.614489	0.461449	0.046145
19	1.1E+06	109594.1	10959.41	1095.9	109.6	11.0	1.095941	0.109594	0.010959
20	2.6E+05	26093.84	2609.384	260.9384	26.09384	2.609384	0.260938	0.026094	0.002609

Sampling Noise



Sampling noise from all stages must be referred back to input !

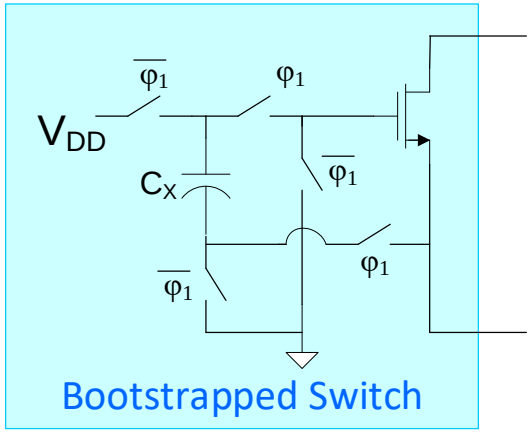
$$v_{INRMS}^2 = v_{IN1}^2 + \frac{1}{A_1^2} v_{IN2}^2 + \frac{1}{A_1^2 A_2^2} v_{IN3}^2 + \ldots + \frac{1}{A_1^2 A_2^2 \cdots A_{n-1}^2} v_{INn}^2$$

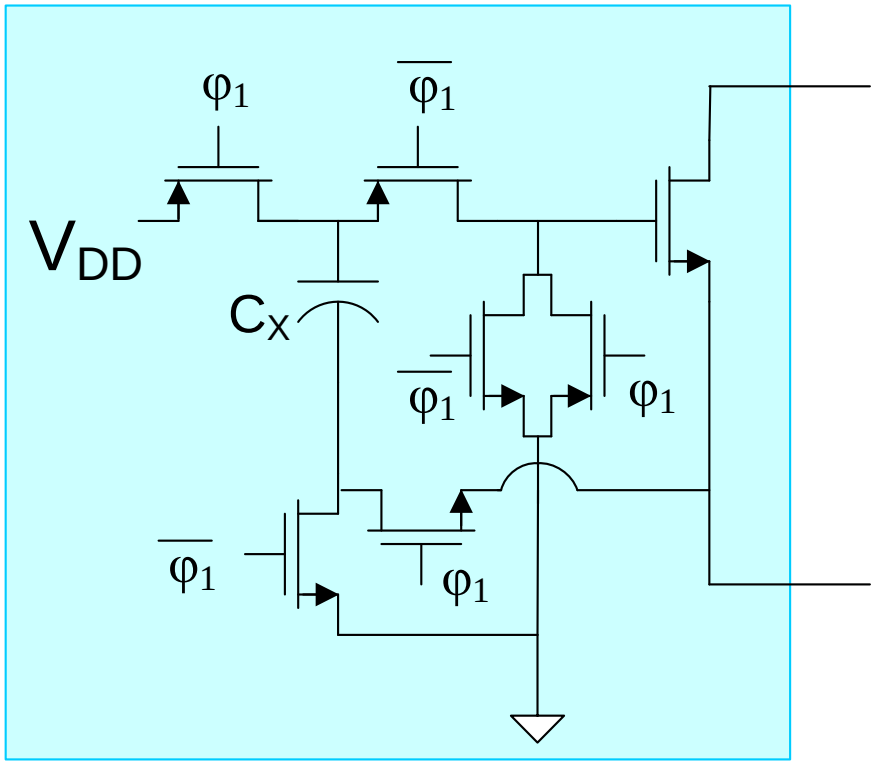
$$v_{INRMS} = \sqrt{v_{IN1}^2 + \sum_{k=2}^{n} \left(\frac{v_{INk}}{\prod_{i=1}^{k-1} A_i} \right)^2}$$

See Katyal,Lin and Geiger, ISCAS, for capacitor sizing for minimization of noise and power

Bootstrapped Switch

Bootstrapping Principle





Conceptual Realization

- May have difficult time turning on some switches
- May stress gate oxide !

Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used,scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.
5. Choice of FB Amplifier Architecture seriously impacts performance	5. Bottom plate sampling, bootatrapping, clock advance to reduce aperature uncertainty,critical GB, parasitic insensitivity needed, β dependent upon architecture and phase, compensation for worst-case β, TG if needed
6. Correct interpretation of α_k's is critical	6. a) Accurately set α_k values b) Use analog or digital calibration

Pipelined Data Converter Design Guidelines

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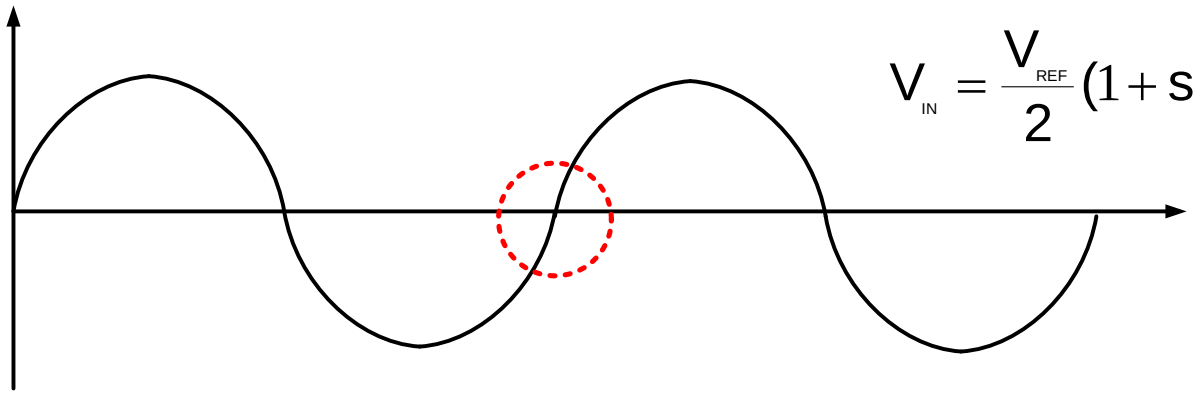
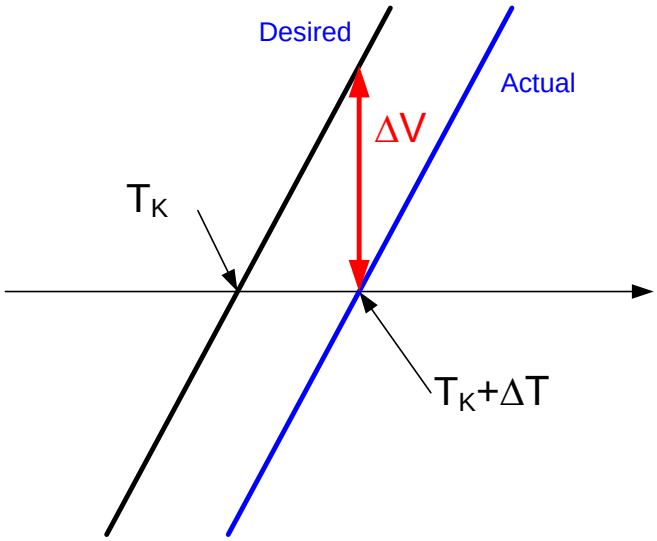
7. Sampling operation inherently introduces a sampled-noise due to noise in resistors	7. Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage) .
8. Signal-dependent tracking errors at input introduce linearity degradation	8. Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches

Aperture Uncertainty



$$V_{IN} = \frac{V_{REF}}{2}(1 + \sin\omega t)$$



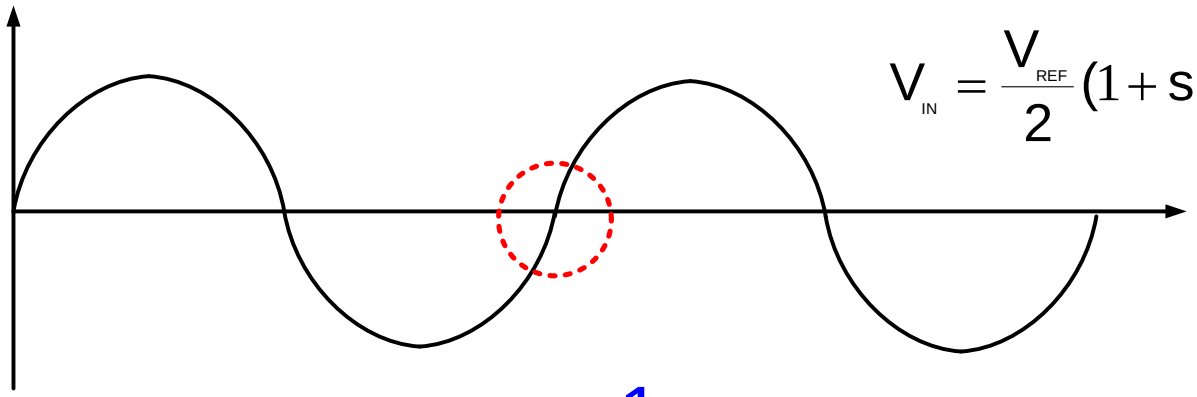
$$\frac{\partial V_{IN}}{\partial t} = \frac{V_{REF}}{2}\omega\cos\omega t)$$

$$\left.\frac{\partial V_{IN}}{\partial t}\right|_{MAX} = \frac{V_{REF}}{2}\omega$$

$$\Delta T < \frac{\Delta V_{MAX}}{\left.\frac{\partial V_{IN}}{\partial t}\right|_{MAX}} = \frac{V_{REF}/2^{n+1}}{\omega V_{REF}/2}$$

$$\Delta T < \frac{1}{\omega 2^{n}}$$

Aperture Uncertainty



$$V_{IN} = \frac{V_{REF}}{2}(1 + \sin\omega t)$$

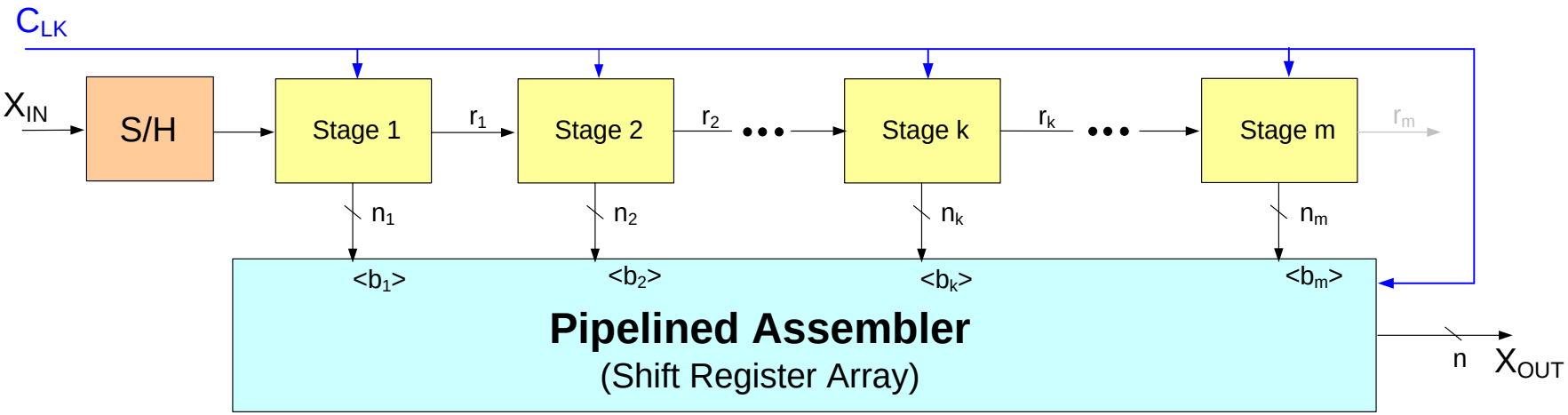
$$\Delta T < \frac{1}{\omega 2^n}$$

Example: If f_{CLK}=200MHz, n=14 determine the aperture uncertainty

$$\Delta T < \frac{1}{2\pi(2E8)2^{14}} = 4.86E\text{-}14 \cong .05\text{psec}$$

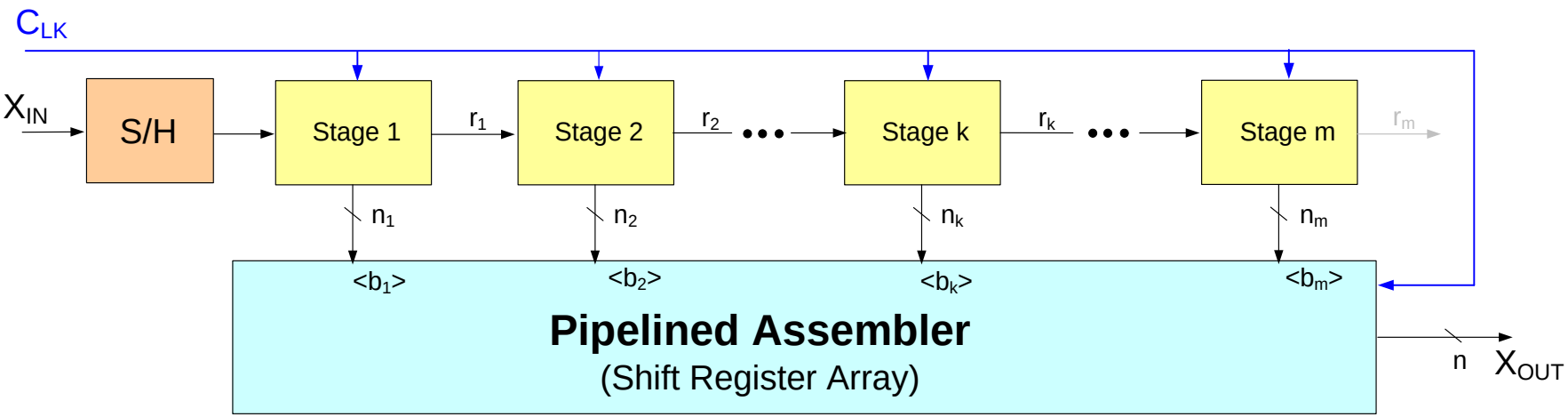
Aperture uncertainty requirements can be very stringent !

Elimination of Input S/H



Why is input S/H used?

Elimination of Input S/H



Why is input S/H used?

Conventional Wisdom:

Because want right sample at input
Because gain stages mess up when input is time varying

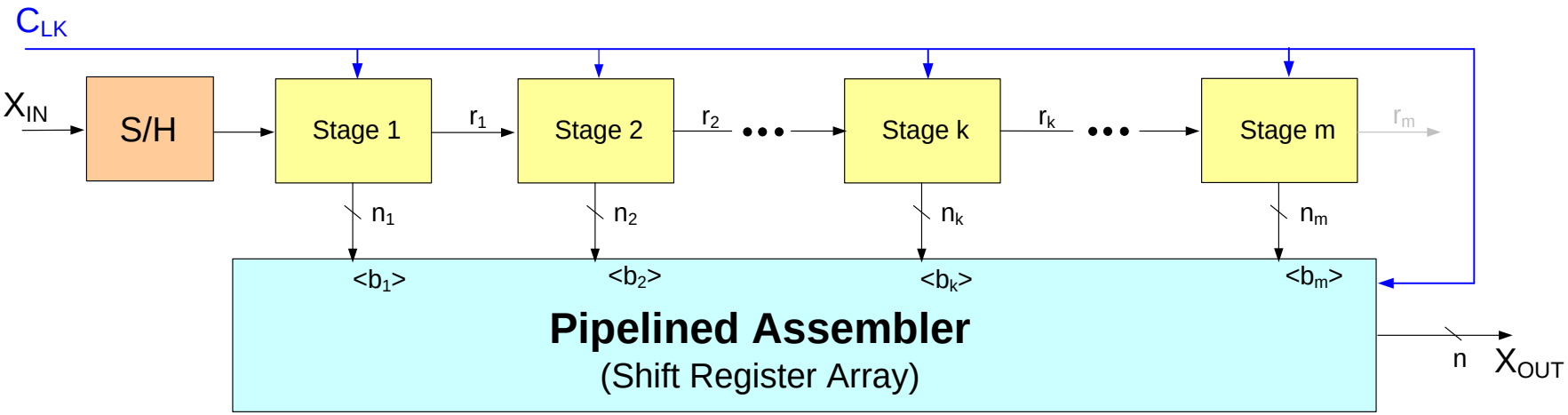
But what does an ADC error do to the Boolean output?

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

Absolutely nothing if over-range protection is provided !

But do need correct value of V_{IN} when creating the residues !!

Elimination of Input S/H



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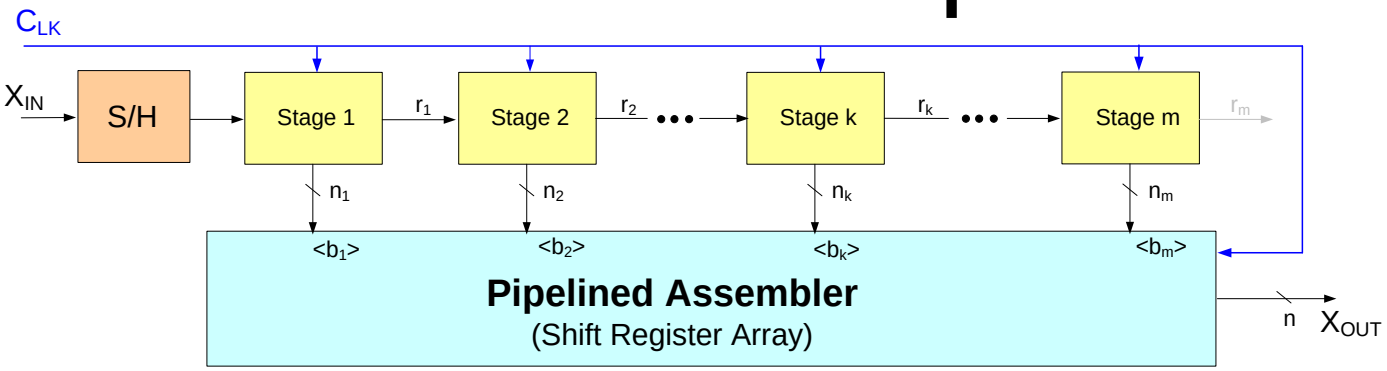
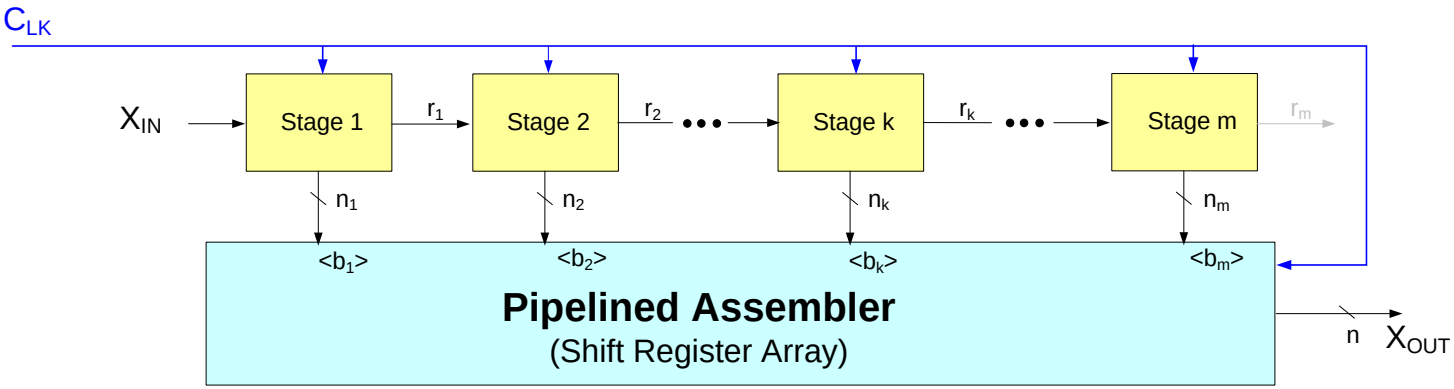
Observation: If SC structures used for the gain stages, there is an inherent sampling that takes place at the input of each stage – including the first stage

Elimination of Input S/H





Advance sampling clock a little so that sample is taken at quiet time but not too much to loose over-range protection

- This simply skews the sampling times
- Probably need to bootstrap the <u>input</u> sampling switch
- Bottom plate sampling

Fully Differential Architectues

Second-order spectral component is often most significant contributor to SFDR and THD limitations in single-ended structures

Noise from ADC and other components, coupled through the substrate, often source of considerable noise in an ADC

- All even-ordered spectral components are eliminated with fully-differential symmetric structures
- Common mode noise is rejected with fully-differential symmetric structures

Almost all implementations of Pipelined ADCs are fully-differential

Straightforward modification of the single-ended concepts discussed here

Authors often present structures in single-ended mode and then just mention that differential structure was used

Modest (but small) increase in area and power for fully differential structures

Signal level increases by factor of 2 and device noise typically increases by $\sqrt{2}$ as well

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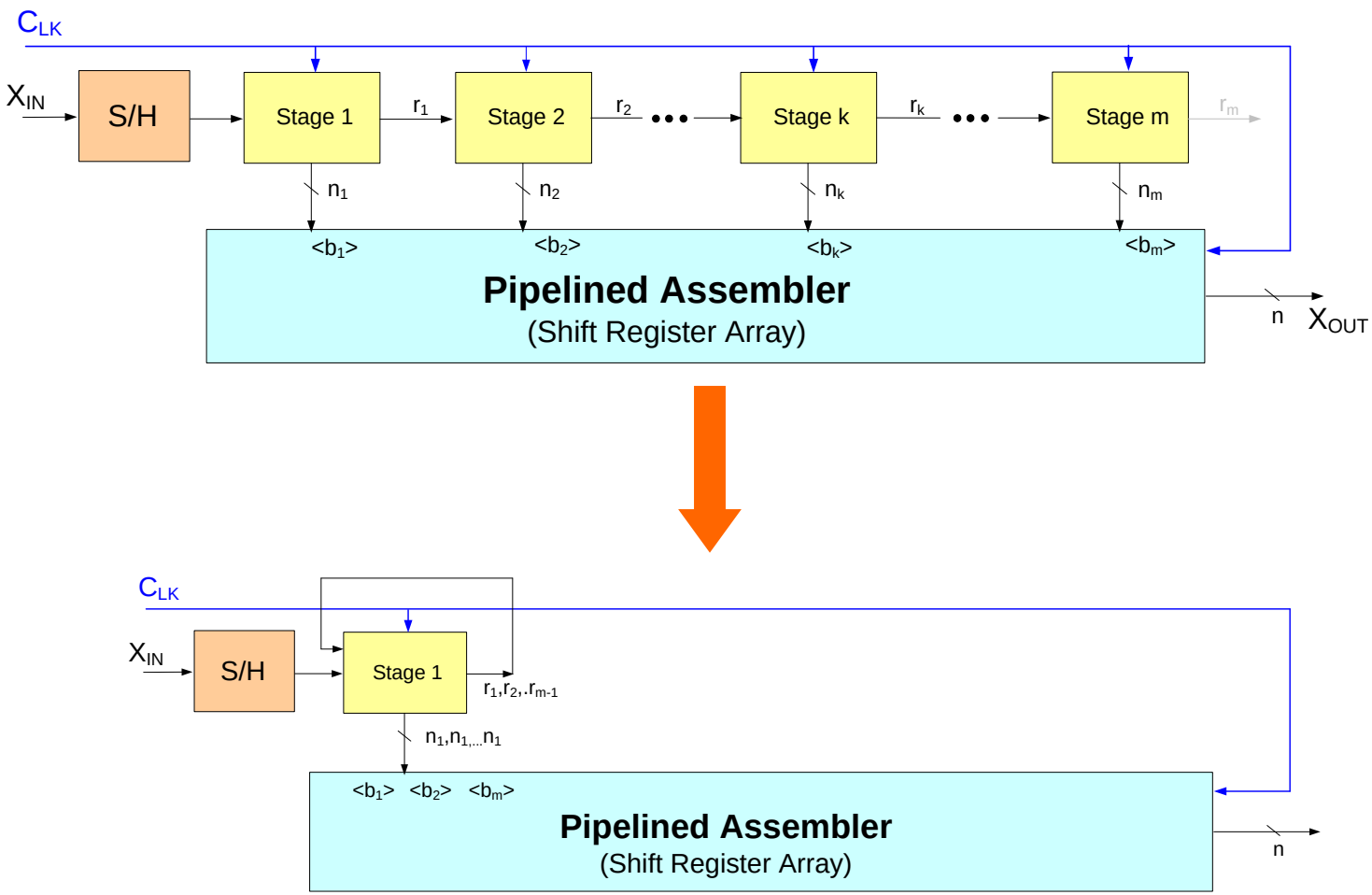
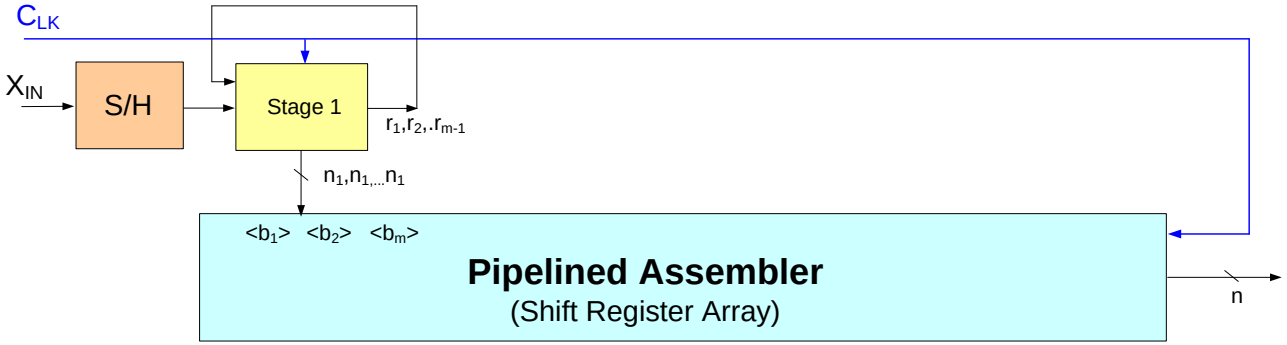
8. Signal-dependent tracking errors at input introduce linearity degradation	8. Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches
9. Aperature uncertainty can cause serious errors	9. Since latency usually of little concern, be sure that a clean clock is used to control all sampling.
10. Input S/H major contributor to nonlinearity and power dissipation	10. Eliminate S/H but provide adequate over-range protection for this removal. Reduces power dissipation and improves linearity!
11. Data converters often have stringent SNR and SNDR requirements	11. Use fully differential structures to obtain dramatic improvements in SNR and SNDR

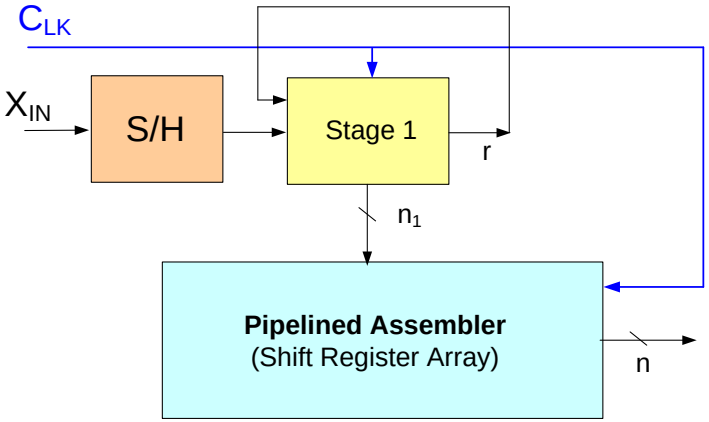
Cyclic (Algorithmic) ADCs

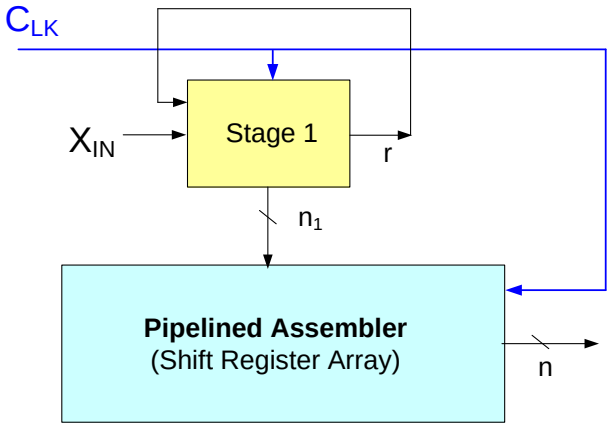


Cyclic (algorithmic) ADC
Reduces throughput but also area

Cyclic (Algorithmic) ADCs

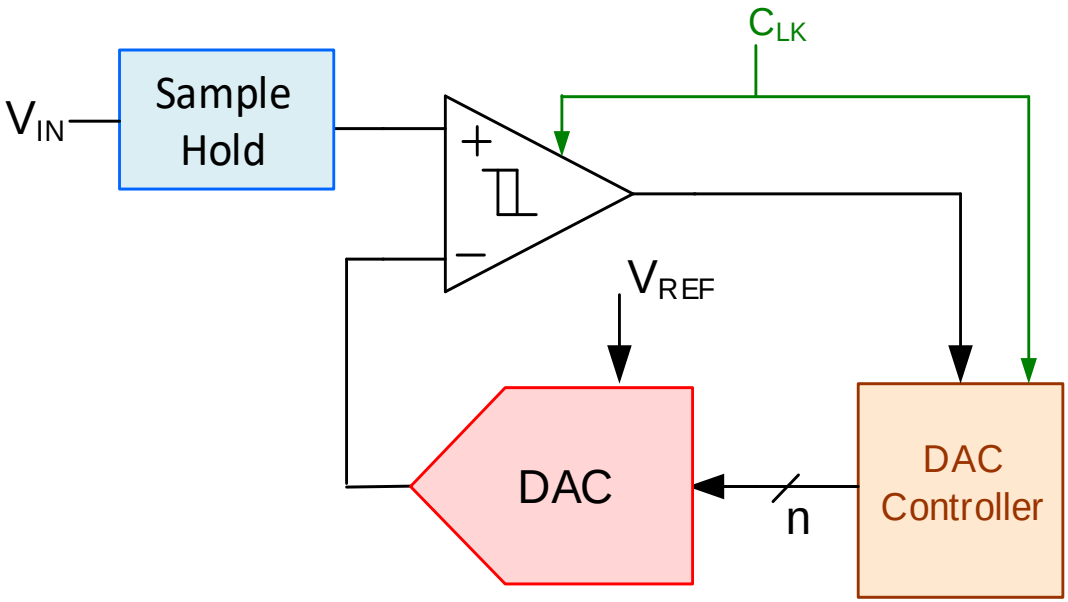






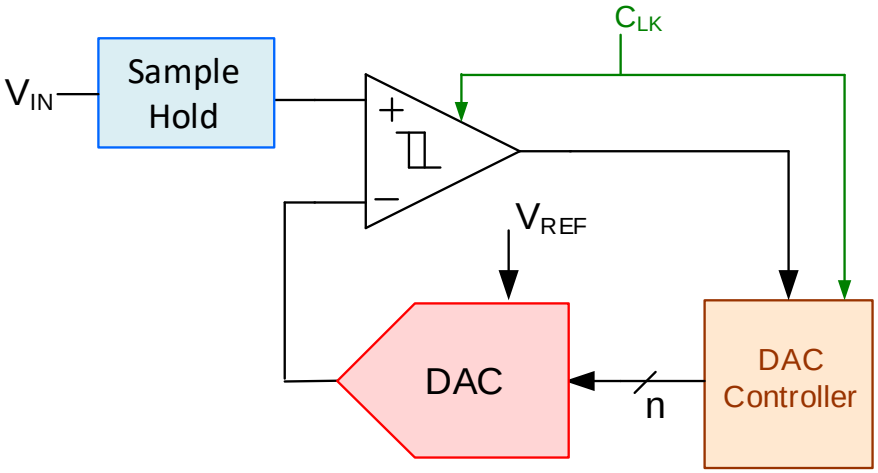
Can bypass bootstrap after initial sample is taken

SAR ADC



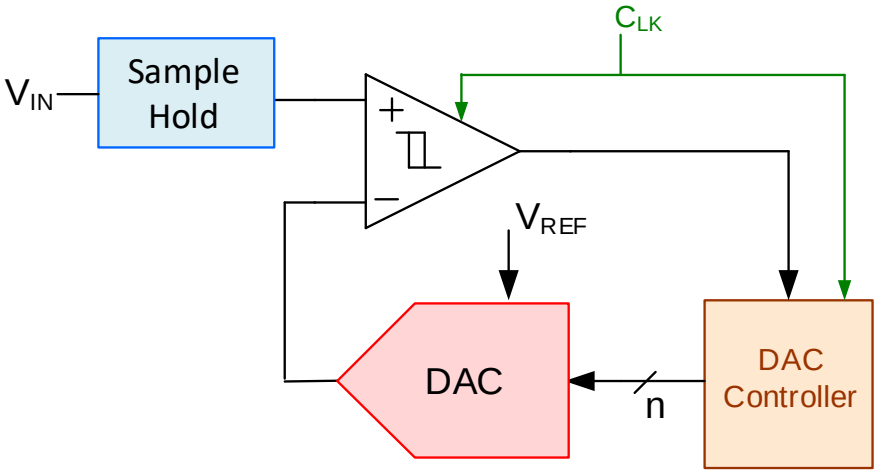
- DAC Controller stores estimates of input in Successive Approximation Register (SAR)
- At end of successive approximation process, ADC output is in SAR
- Eliminates the power-consuming amplifiers of the pipelined ADC
- Much slower than pipelined ADC
- S/H at the input is essential
- Can have excellent power performance
- Widely used structure with renewed attention in recent years

SAR ADC



- Any DAC structure can be used
- In basic structure, single comparator can be used
- Performance entirely determined by S/H, DAC, and comparator
- Very simple structure and relatively fast design procedure
- If offset voltage of comparator is fixed, comparator offset will not introduce any nonlinearity

SAR ADC



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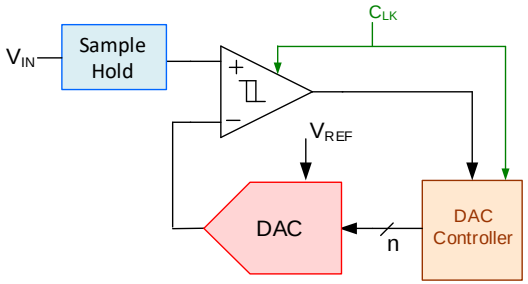
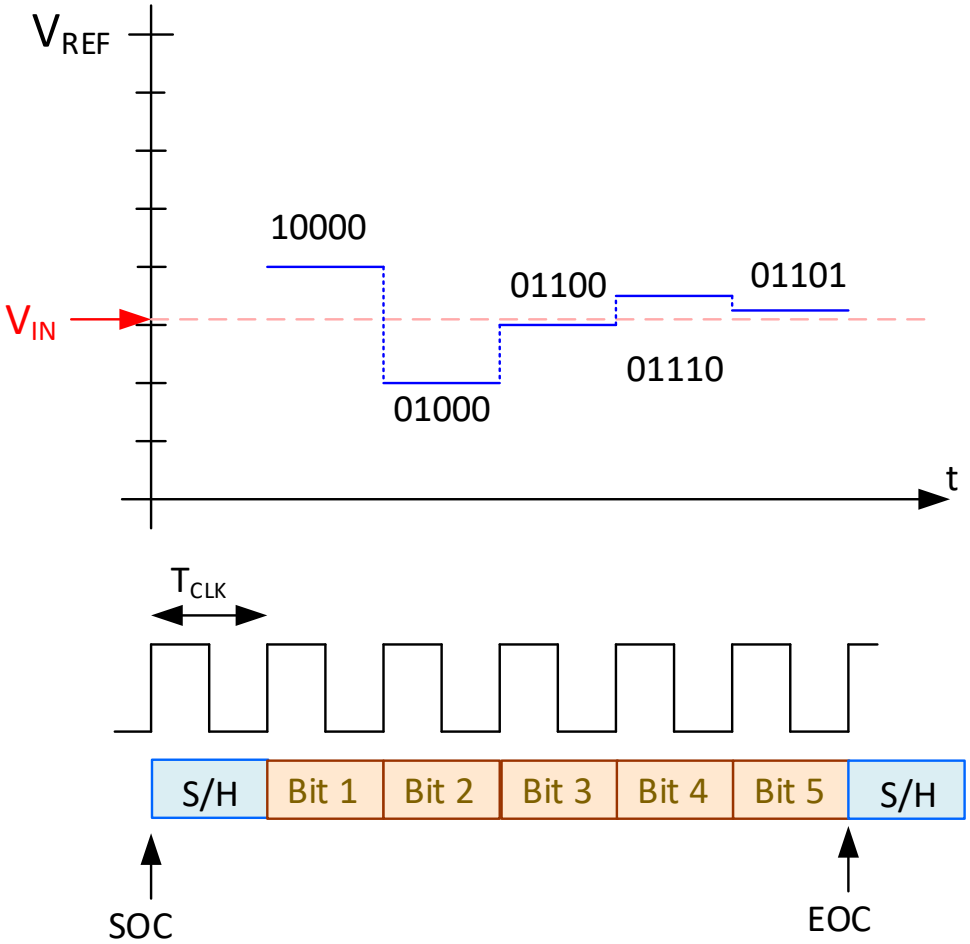
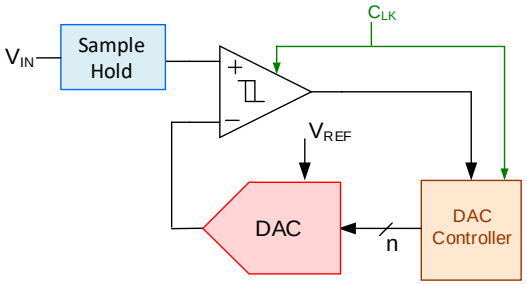


Typical Operation (shown for 5 bits)

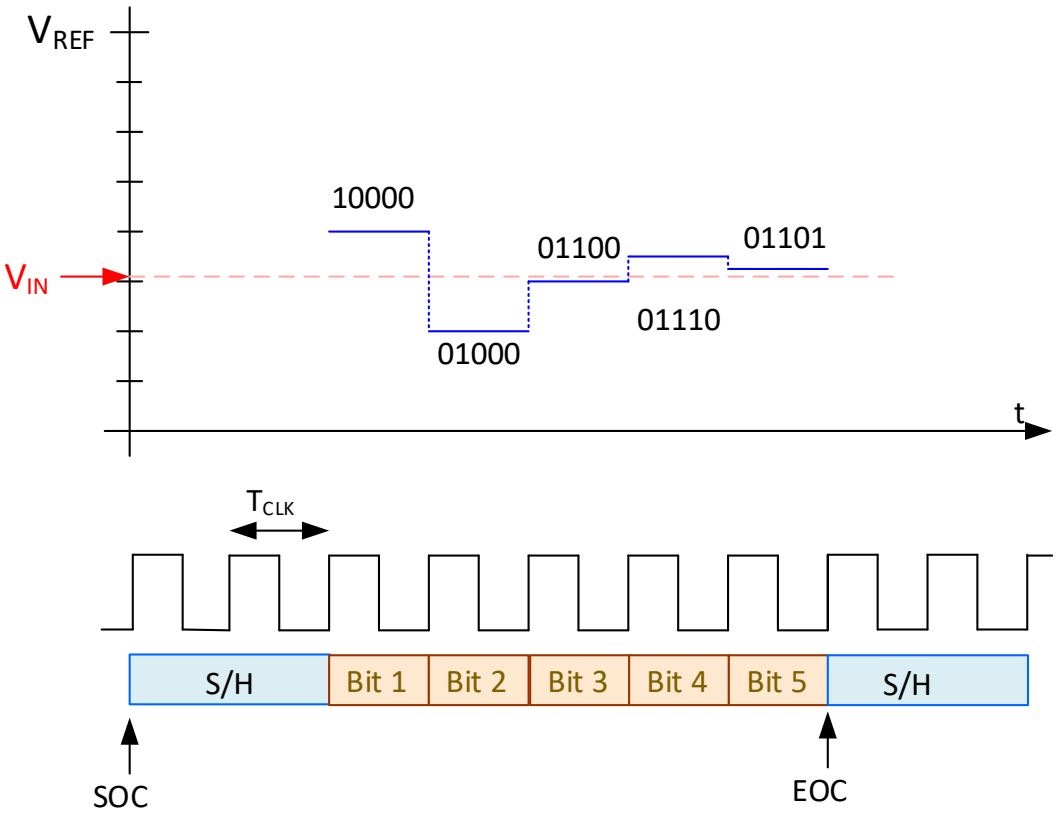


- Requires n+1 clock cycles
- Can be extended to large number of bits (16 or more)
- Comparator requires large CM range
- Speed limited by S/H

SAR ADC

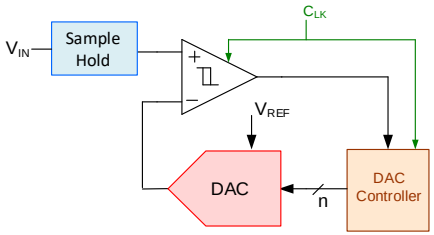


Typical Operation (shown for 5 bits)

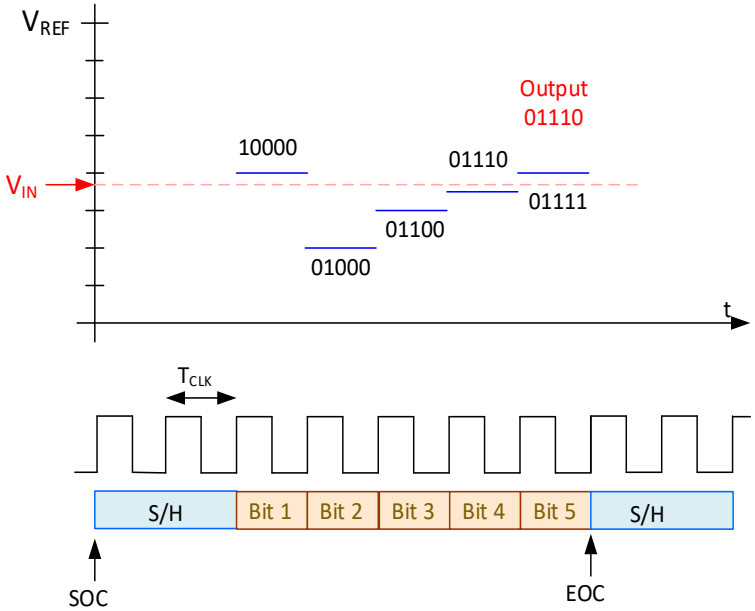


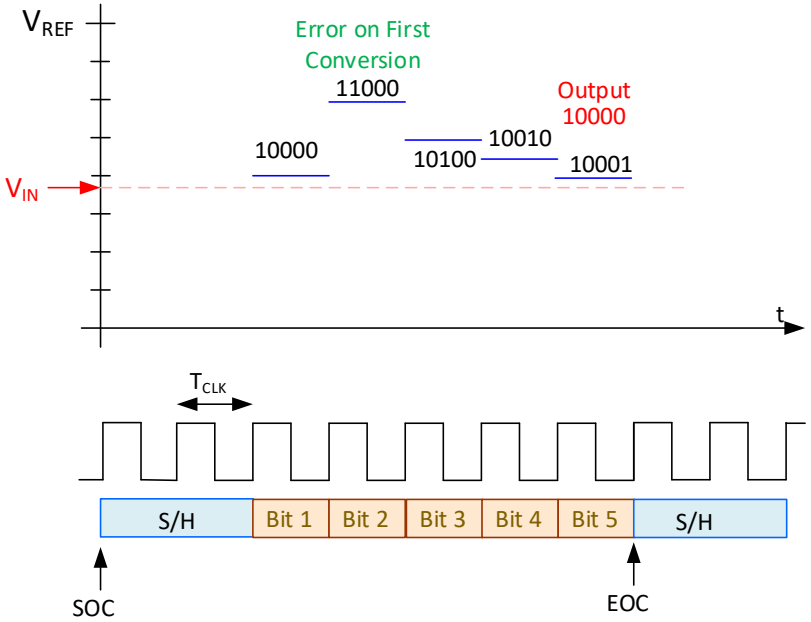
- Two or more bit periods can be added to S/H
- Slows overall operation proportionally but overhead small for large n

SAR ADC



- Does not recover from errors
- Particularly problematic when errors occur on earlier bits
- Over-range protection can be added but at expense of additional clock periods





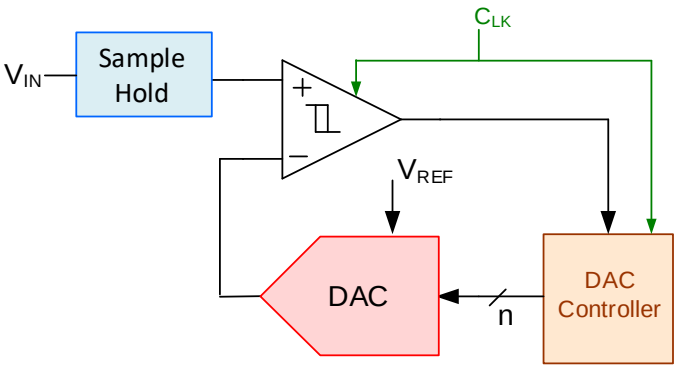
SAR ADC

Note notation difference

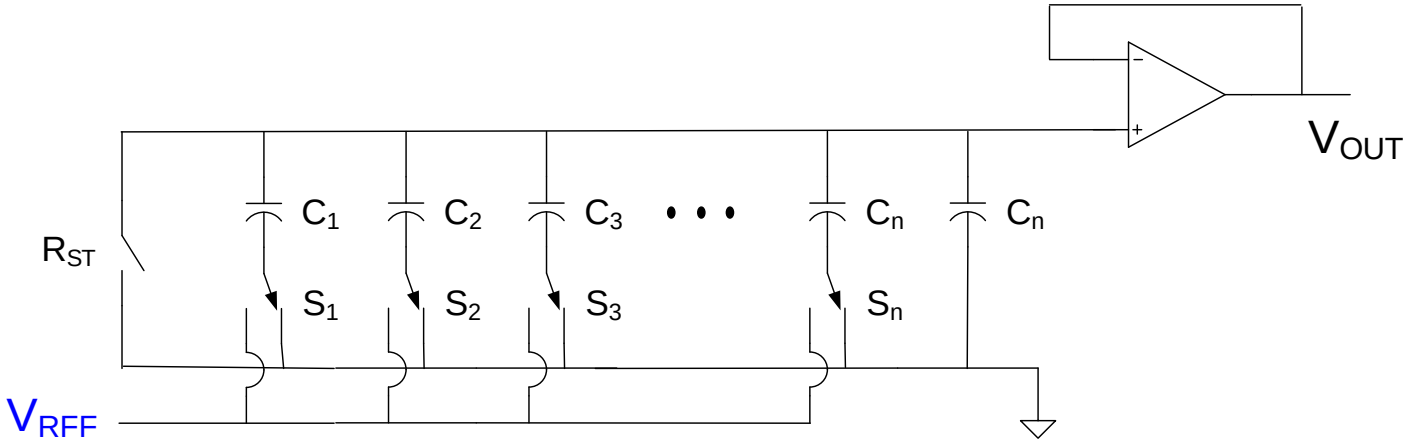
$\vec{X}_{OUT}=<d_{n-1},d_{n-2},\ldots d_0>$

d_0 is the Least Significant Bit (LSB)

d_{n-1} is the Most Significant Bit (MSB)

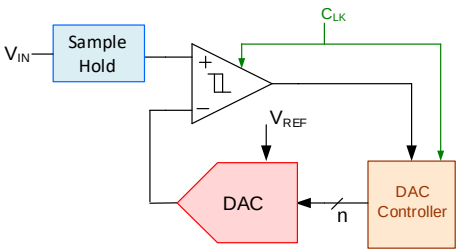


Charge Redistribution DAC could be used in SAR ADCs

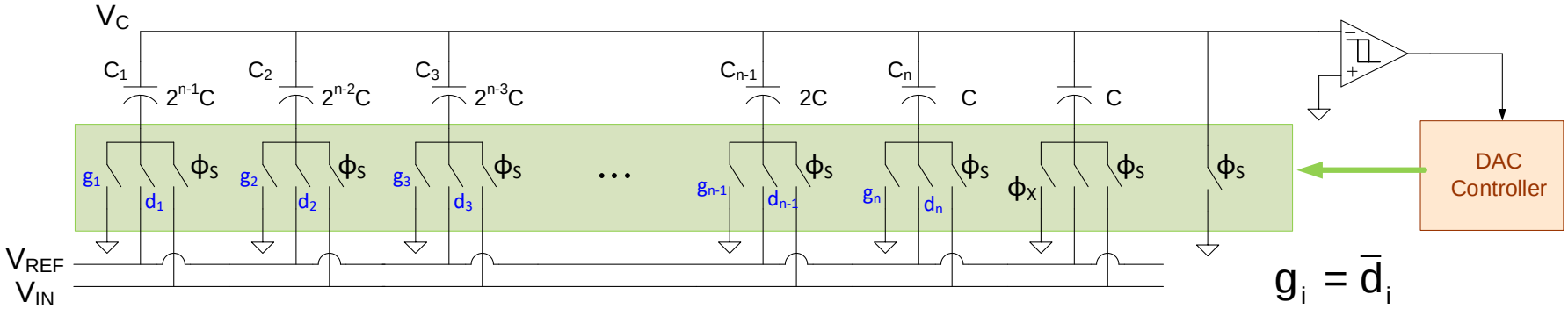


- Capacitors usually binary weighted
- With this DAC, typical common-mode input required for comparator
- Standard S/H also required

SAR ADC

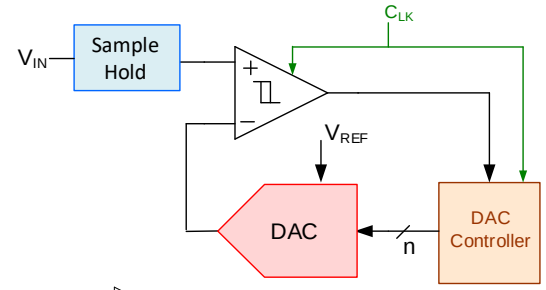


Alternate Charge Redistribution DAC

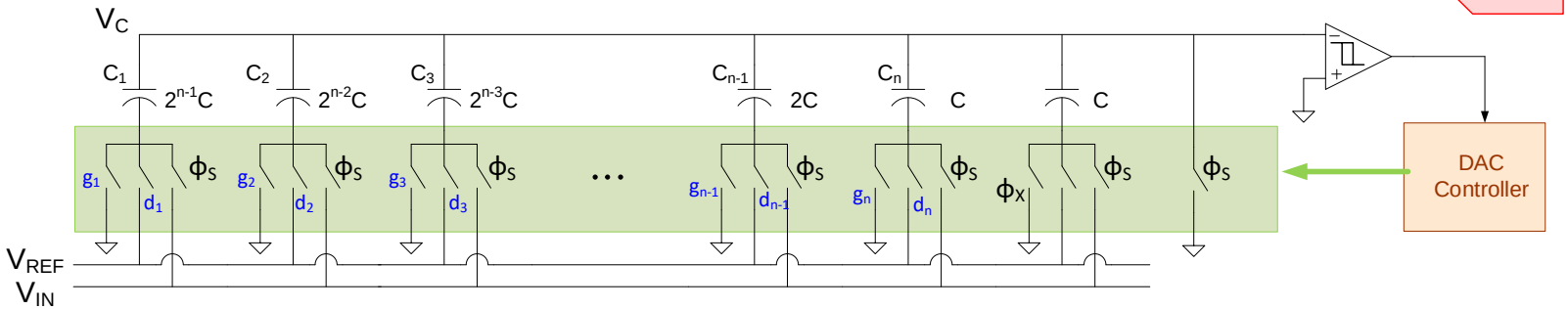


- During sampling phase, input is sampled on all capacitors
- During successive approximation process, capacitors are alternately connected to ground or V_{REF}
- Voltage on common node will converge to 0
- Comparator is always comparing to ground thus reducing common-mode nonlinearity errors
- Note input sample is <u>not</u> held independently throughout the entire conversion process
- Bootstrapped switch is critical during sampling phase
- Parasitic capacitances on V_C node do not affect final output (Bottom plate)
- Major source of power dissipation is in the charge redistribution process

SAR ADC



Alternate Charge Redistribution DAC



$$C_i = C2^{n-i} \qquad 1 \le i \le n$$

Define Q to be the charge sampled onto capacitors $Q = Q_{SAMP}$ and define $g_i = \bar{d}_i$ and $\phi_X = \bar{\phi}_S$

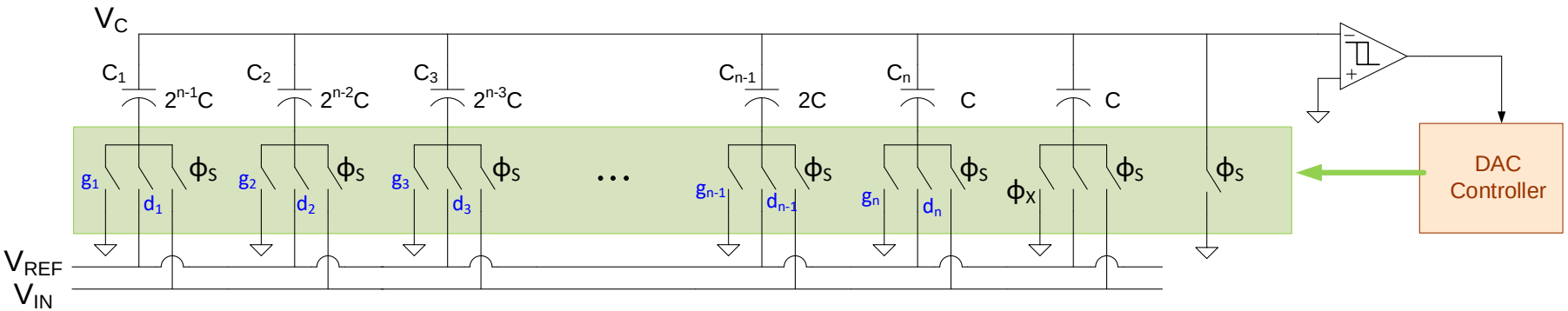
$$\left.\begin{aligned} Q &= 2^n C V_{IN} \\ Q &= \sum_{i=1}^{n} C_i \left(d_i V_{REF} - V_C\right) - C V_C \end{aligned}\right\}$$

$$Q = \sum_{i=1}^{n} C2^{n-i}\left(d_i V_{REF} - V_C\right) - CV_C = CV_{REF}\sum_{i=1}^{n} d_i 2^{n-i} - CV_C\left(\sum_{i=1}^{n} 2^{n-i} + 1\right)$$

$$\Rightarrow \quad Q = CV_{REF}\sum_{i=1}^{n} d_i 2^{n-i} - CV_C\left(2^n\right)$$

SAR ADC

Alternate Charge Redistribution DAC



$$CV_{REF}\sum_{i=1}^{n} d_i 2^{n-i} - CV_C\left(2^n\right) = 2^n CV_{IN}$$

$$V_{IN} = V_{REF}\sum_{i=1}^{n} d_i \frac{2^{n-i}}{2^n} - V_C$$

$$V_{IN} = V_{REF}\sum_{i=1}^{n} d_i 2^{-i} - V_C$$

If the SAR output is adjusted so that

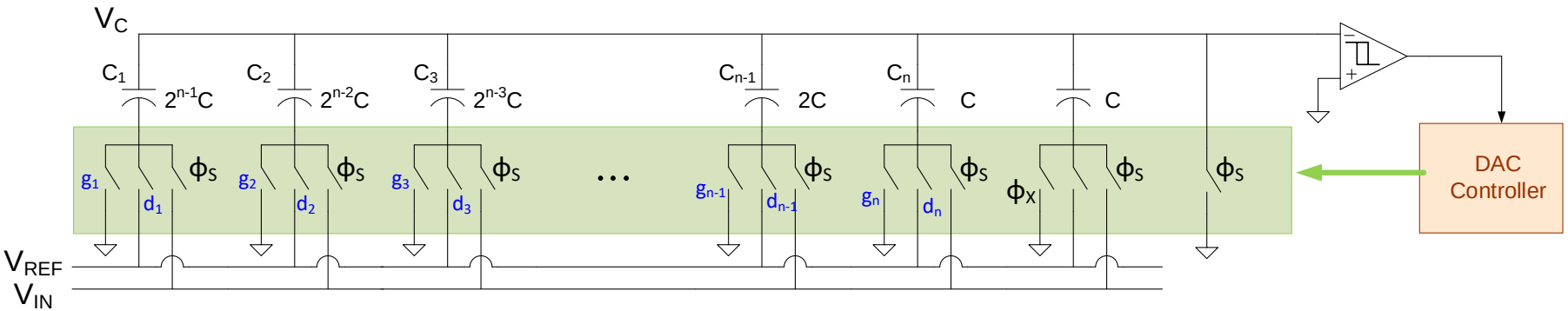
$$-\frac{V_{REF}}{2^n} \le V_C \le \frac{V_{REF}}{2^n}$$

It follows that

$$V_{REF}\sum_{i=1}^{n} d_i 2^{-i} - \frac{V_{REF}}{2^n} \le V_{IN} \le V_{REF}\sum_{i=1}^{n} d_i 2^{-i} + \frac{V_{REF}}{2^n}$$

SAR ADC

Alternate Charge Redistribution DAC



Binary Search Process Description

1. After sampling V_{IN} with φ_S, envision closing all g switches and φ_X V_C will be $-V_{IN}$.
2. Close d_1 It follows that

$$C_1(V_{REF} - V_C) - \sum_{i=2}^{n} C_i V_C - CV_C = \sum_{i=1}^{n} C_i V_{VIN} + CV_{IN}$$

solving obtain $V_C = 2^{-1}V_{REF} - V_{IN}$

thus $V_C > 0 \quad \Rightarrow d_1 = 0$

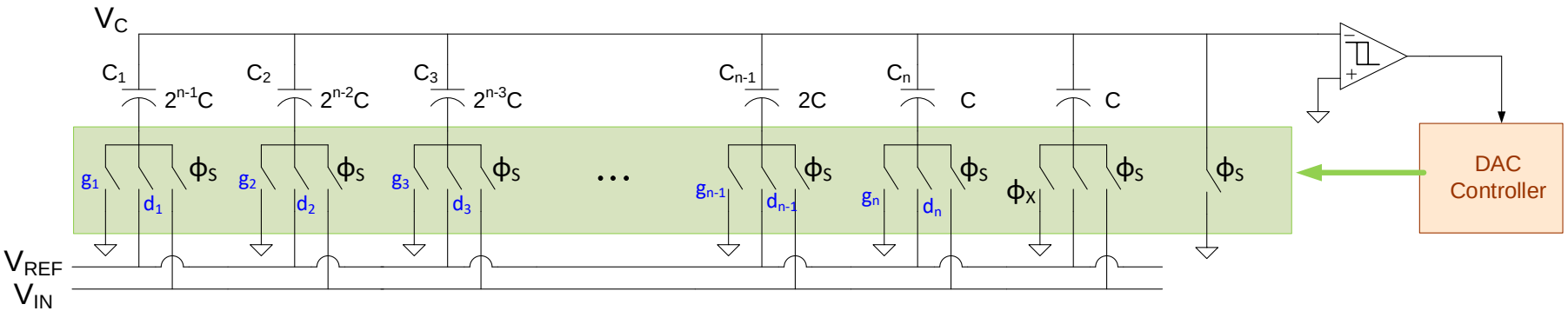
3. Since d_1=0, close g_1 and now close d_2. It follows that

$$V_C = 2^{-2}V_{REF} - V_{IN}$$

thus $V_C < 0 \quad \Rightarrow d_2 = 1$

SAR ADC

Alternate Charge Redistribution DAC



Binary Search Process Description

4. Since d_2=1, leave d_2 closed and now close d_3. It follows that

$$V_C = 2^{-3}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

thus $V_C > 0 \quad \Rightarrow d_3 = 0$

5. Since d_3=0, open d_3 and now close d_4. It follows that

$$V_C = 2^{-4}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

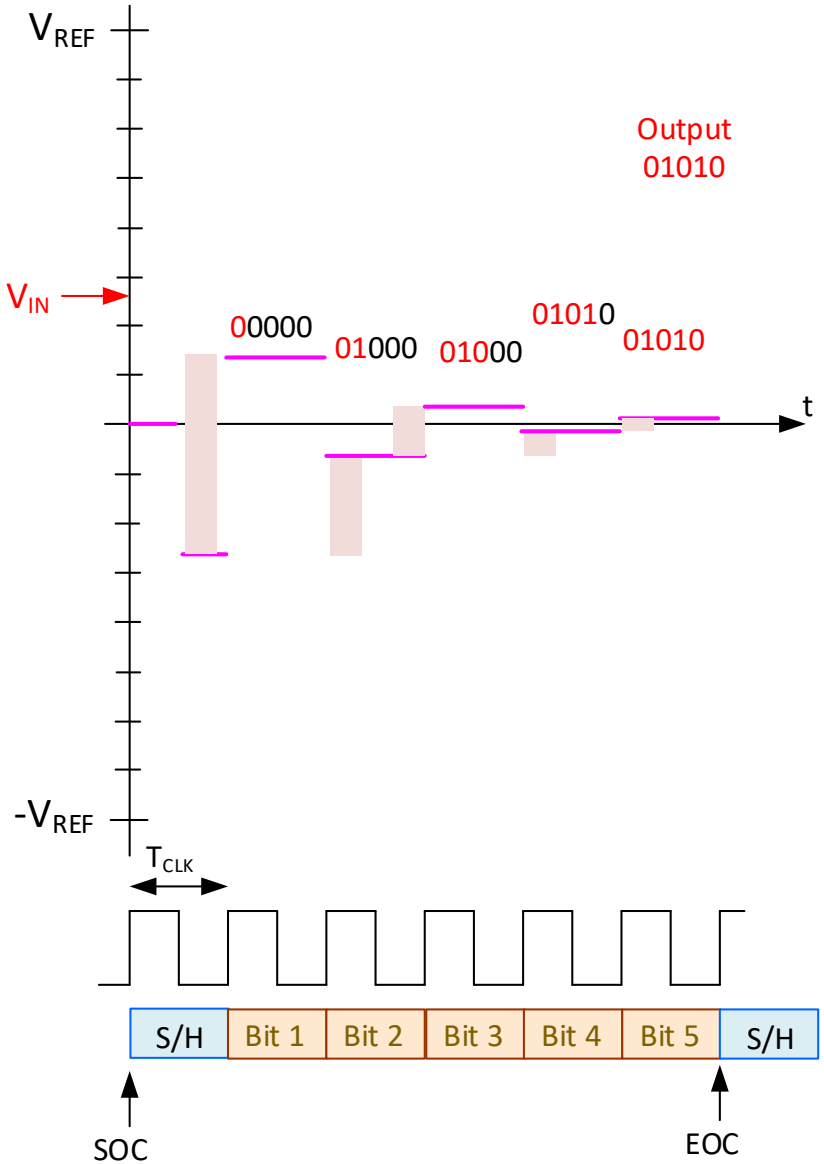
thus $V_C < 0 \quad \Rightarrow d_4 = 1$

6. Since d_4=1, keep d_4 closed and now close d_5. It follows that

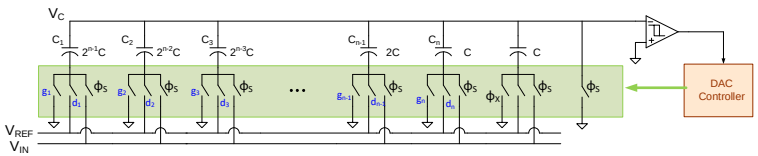
$$V_C = 2^{-5}V_{REF} + 2^{-4}V_{REF} + 2^{-2}V_{REF} - V_{IN}$$

thus $V_C > 0 \quad \Rightarrow d_5 = 0$

SAR ADC

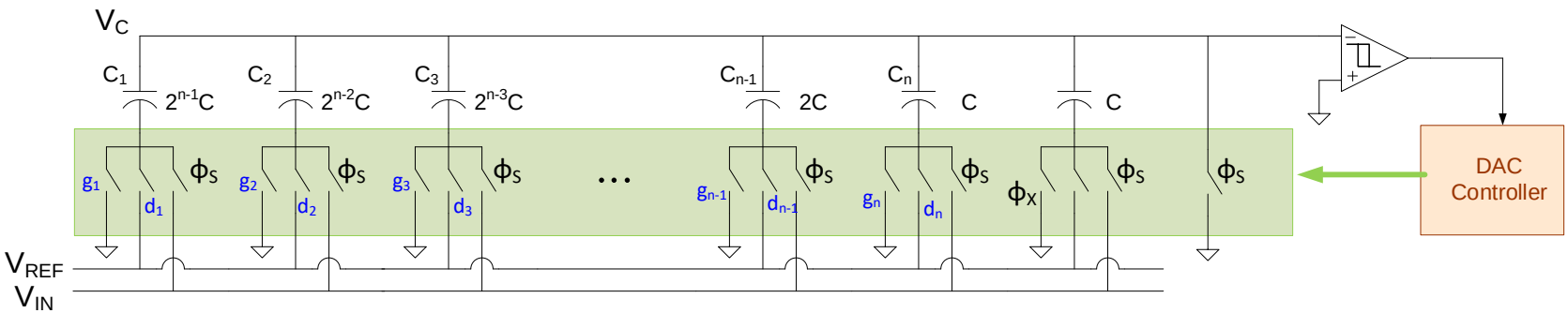


Alternate Charge Redistribution DAC



SAR ADC

C-2C Array for Charge Redistribution DAC



Can a C-2C array be used for the charge-redistribution DAC?

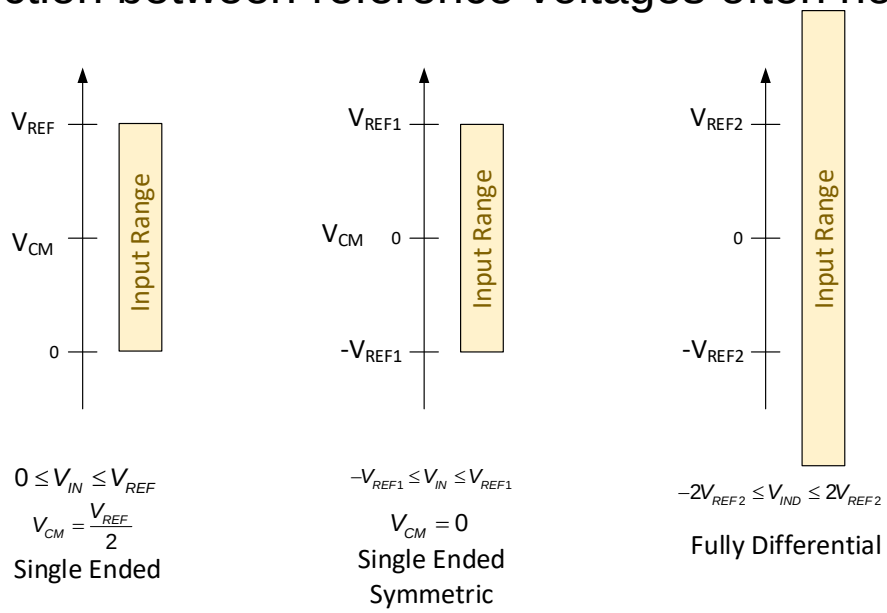
Yes – but internal nodes would all need to settle !

Can a counter be used rather than a binary search to obtain the SAR code?

Yes – but conversion time would be long with worst-case requiring 2^n periods

SAR ADC

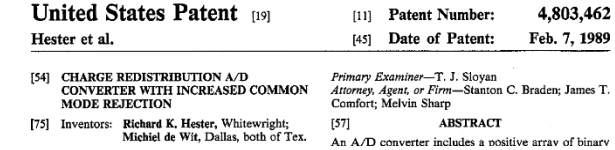
- Concepts are often expressed in single-ended structures
- Fully differential structures widely used
- Distinction between reference voltages often not clearly stated



Is Common-Mode input 0 or $V_{REF}/2$?
Is maximum input V_{REF}, $2V_{REF}$ or $4V_{REF}$:

- Single-ended V_{REF}
- Single-ended Differential Input $+V_{REF}$, $-V_{REF}$
- Differential Input

Example of Fully Differential Implementation



United States Patent [19]
Hester et al.

[11] **Patent Number: 4,803,462**
[45] **Date of Patent: Feb. 7, 1989**

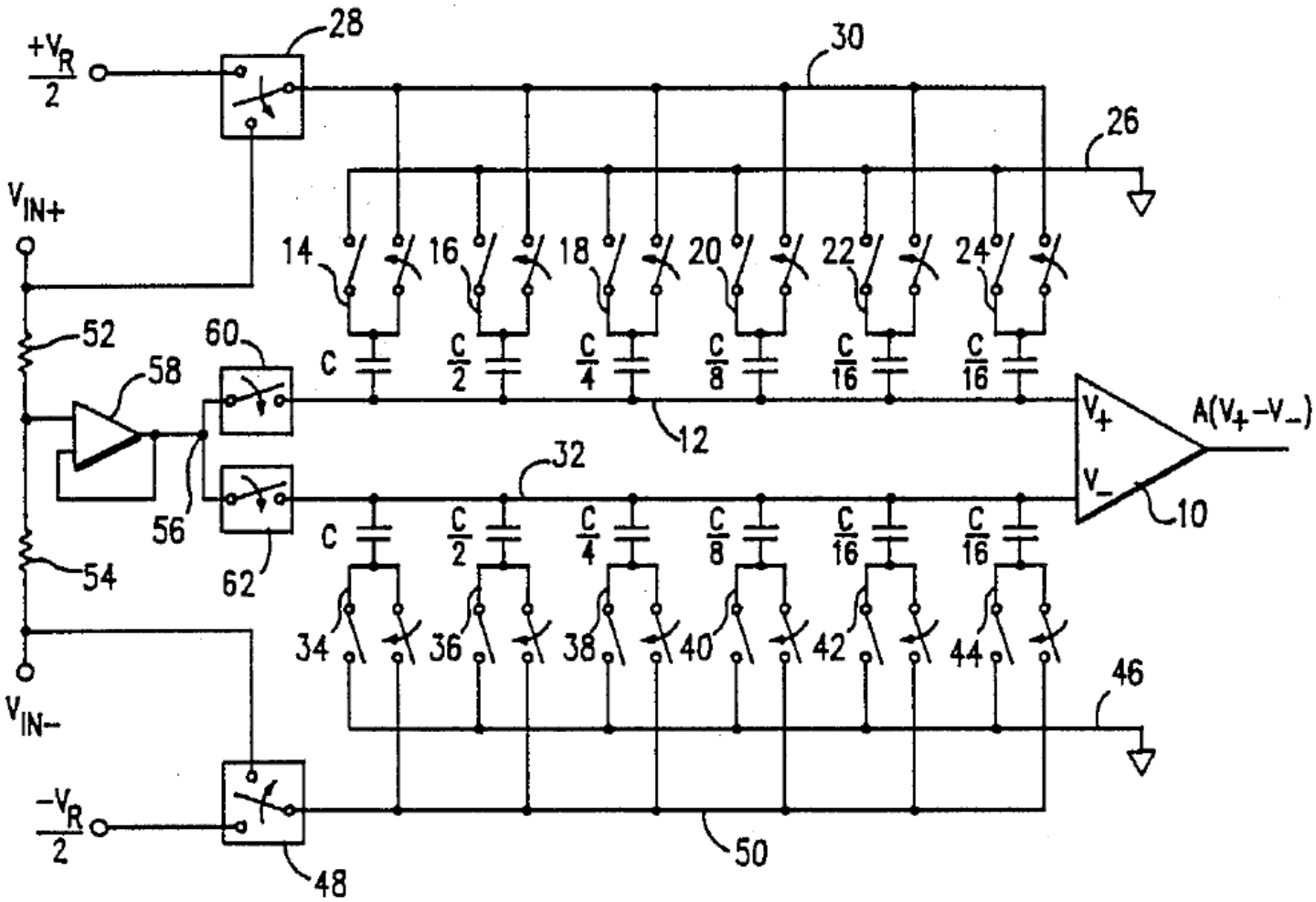
[54] **CHARGE REDISTRIBUTION A/D CONVERTER WITH INCREASED COMMON MODE REJECTION**

[75] Inventors: **Richard K. Hester**, Whitewright; **Michiel de Wit**, Dallas, both of Tex.

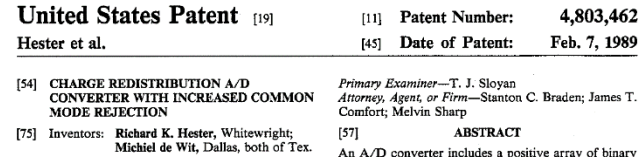
Primary Examiner—T. J. Sloyan
Attorney, Agent, or Firm—Stanton C. Braden; James T. Comfort; Melvin Sharp

[57] **ABSTRACT**

An A/D converter includes a positive array of binary



Another example of Fully Differential Implementation with different switching sequence and different references.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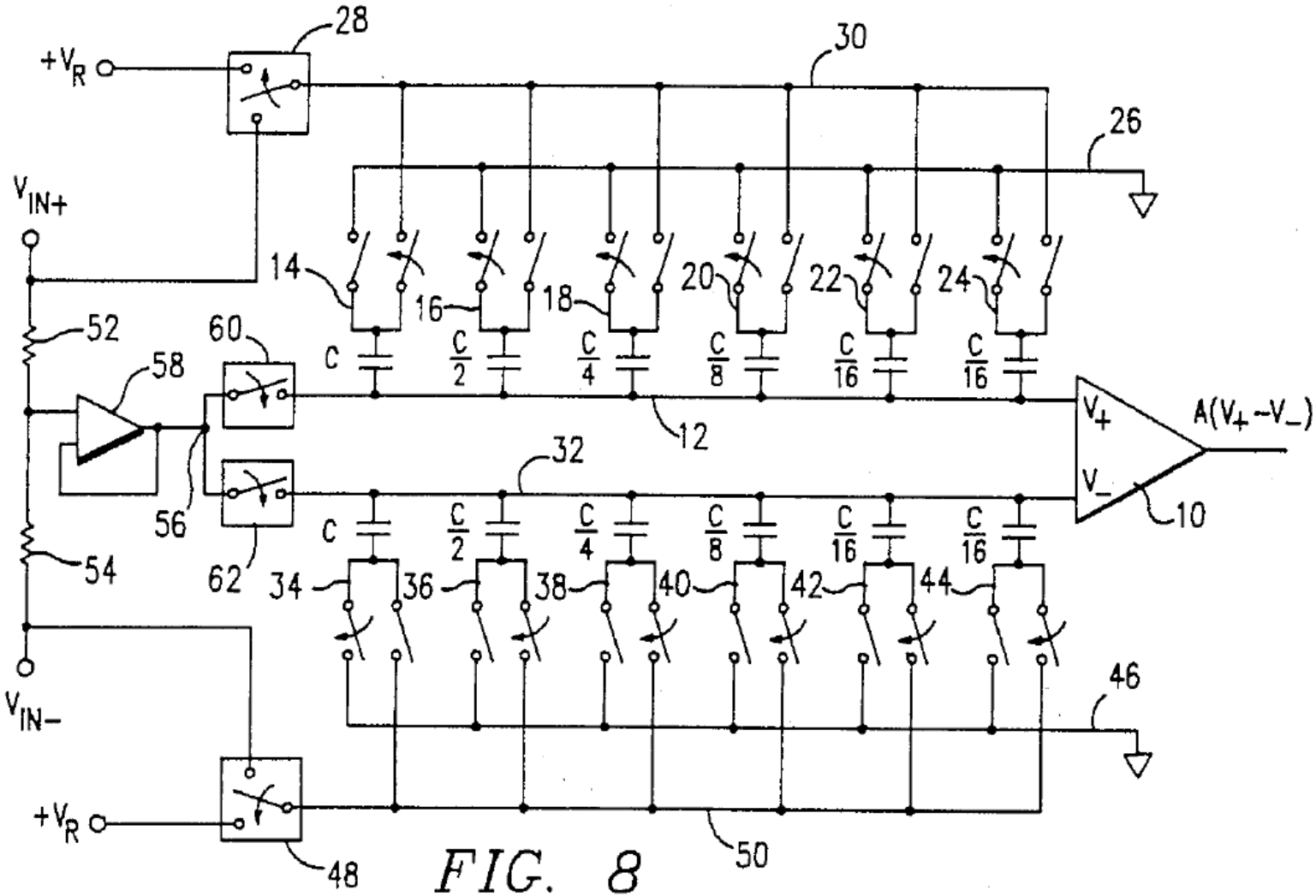

FIG. 8

SAR ADC

Charge Redistribution ADC with reduced charge redistribution energy

Goal: Reduce unnecessary switching inherent in the original process by first switching all capacitors to V_{REF} and then returning to ground if test fails.

[PDF] **A 10-bit** 50-MS/s **SAR ADC** with **a monotonic capacitor** switching procedure

CC Liu, SJ Chang, GY Huang… - IEEE Journal of Solid …, 2010 - msicdt.ee.ncku.edu.tw

This paper presents **a** low-power **10-bit** 50-MS/s suc-cessive approximation register (**SAR**) analog-to-digital converter (**ADC**) that uses **a monotonic capacitor** switching procedure. Compared to converters that use **the** conventional procedure, **the** average switching energy …

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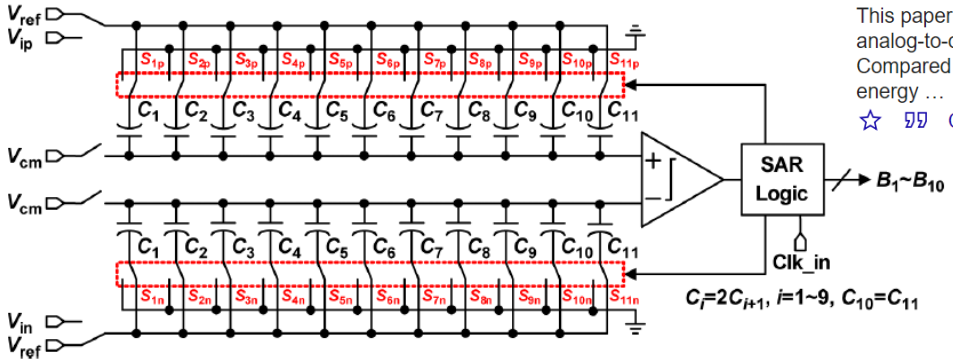
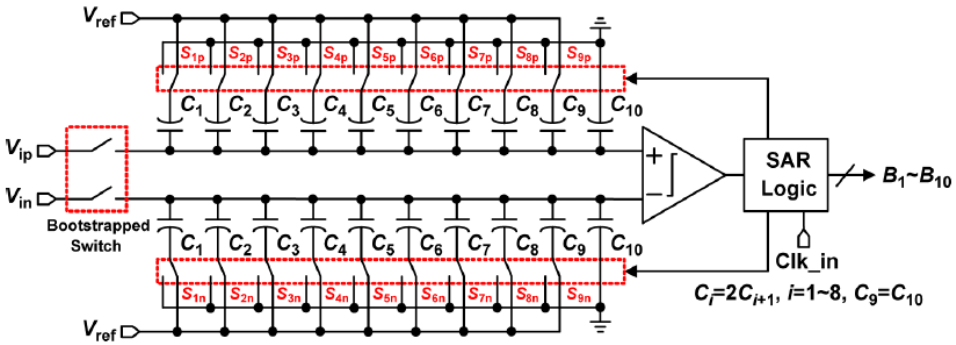
550 (April 2017 I believe)
788 (4/17/2019)

Goal: Only switch if needed!



Standard Switching



Reduced Switching

Samples input on array connected between V_{IN} and V_{REF}

Only change state if output must be decreased

For 10-bit ADC, reported switching energy and total capacitance reduced by about 81% and 50%, respectively

Does not consider kT/C noise since resolution is small

SAR ADC

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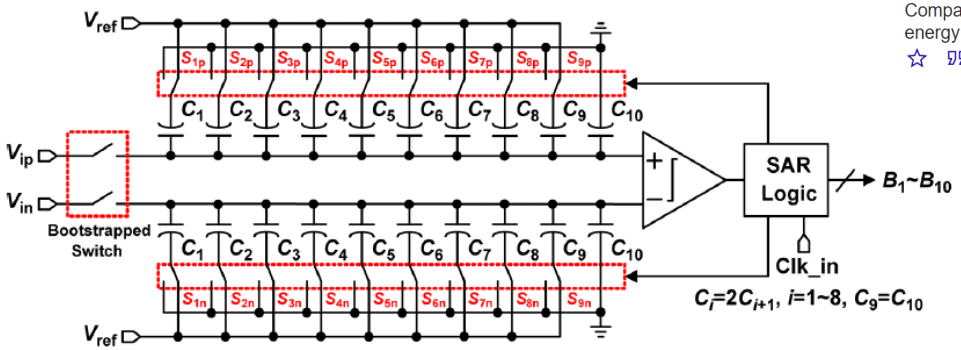
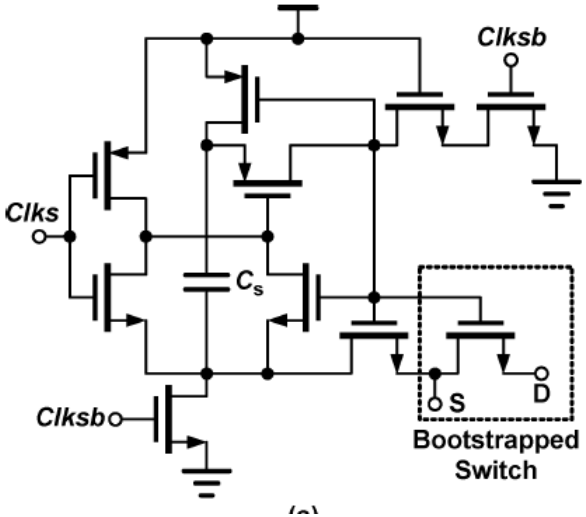
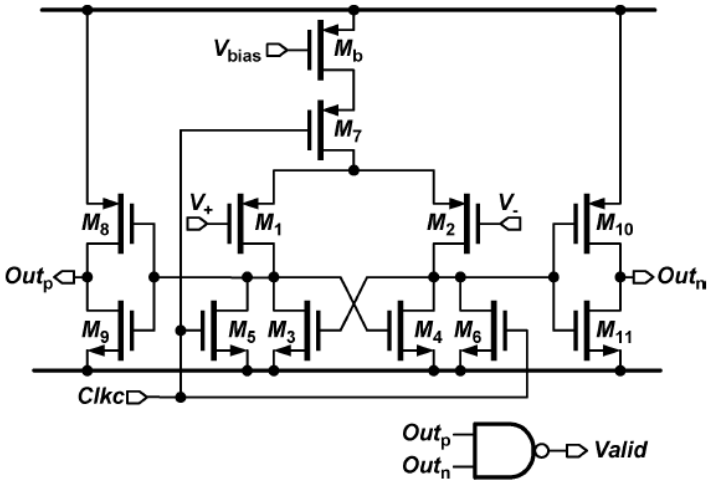
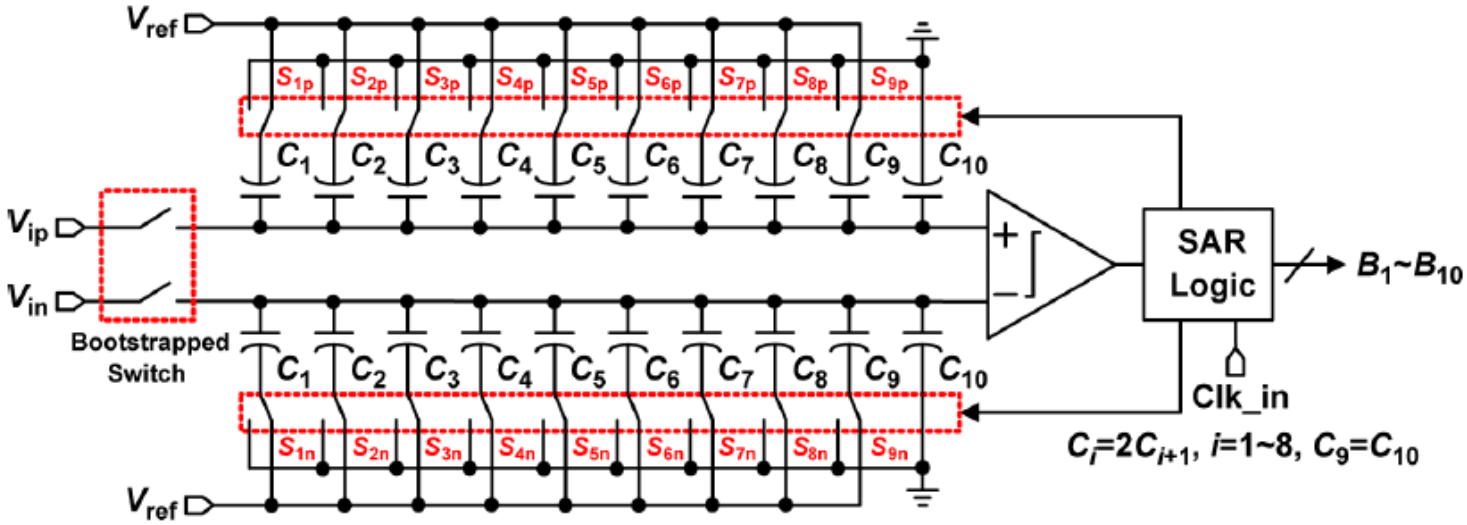
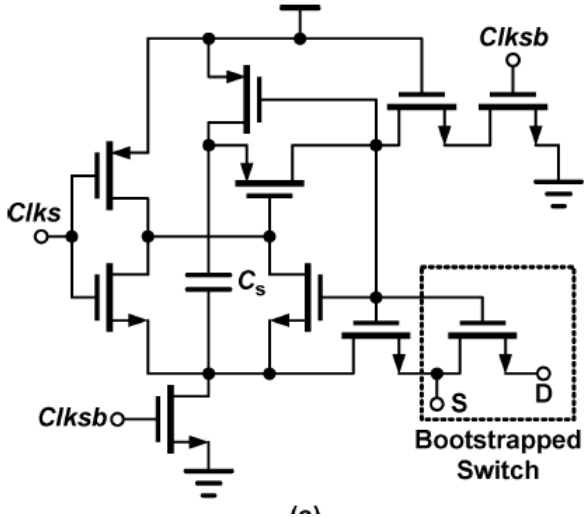


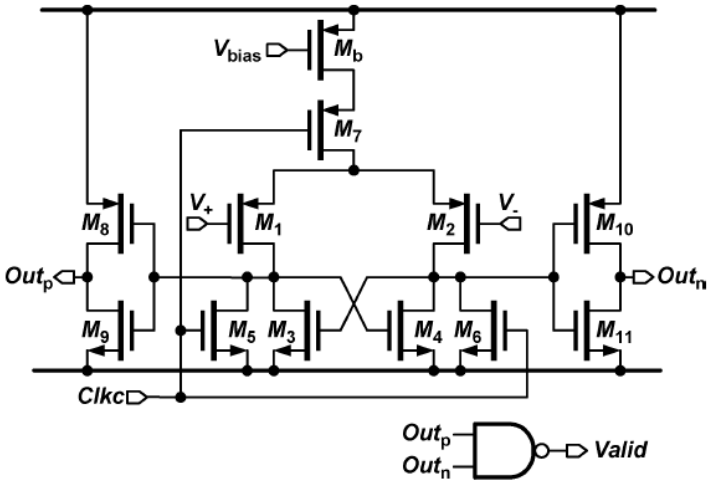




SAR ADC


Vref
S1p S2p S3p S4p S5p S6p S7p S8p S9p
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10
Vip
Vin
Bootstrapped Switch
SAR Logic
B1~B10
Clk_in
S1n S2n S3n S4n S5n S6n S7n S8n S9n
Ci=2Ci+1, i=1~8, C9=C10


Clksb
Clks
Cs
S
D
Bootstrapped Switch


Vbias
Mb
M7
V+
M1
M2
V-
M8
M10
Outp
Outn
M9
M5 M3
M4 M6
M11
Clkc
Outp
Outn
Valid

SAR ADC

Charge Sharing ADC with reduced charge redistribution energy

Goal: Have only passive switching

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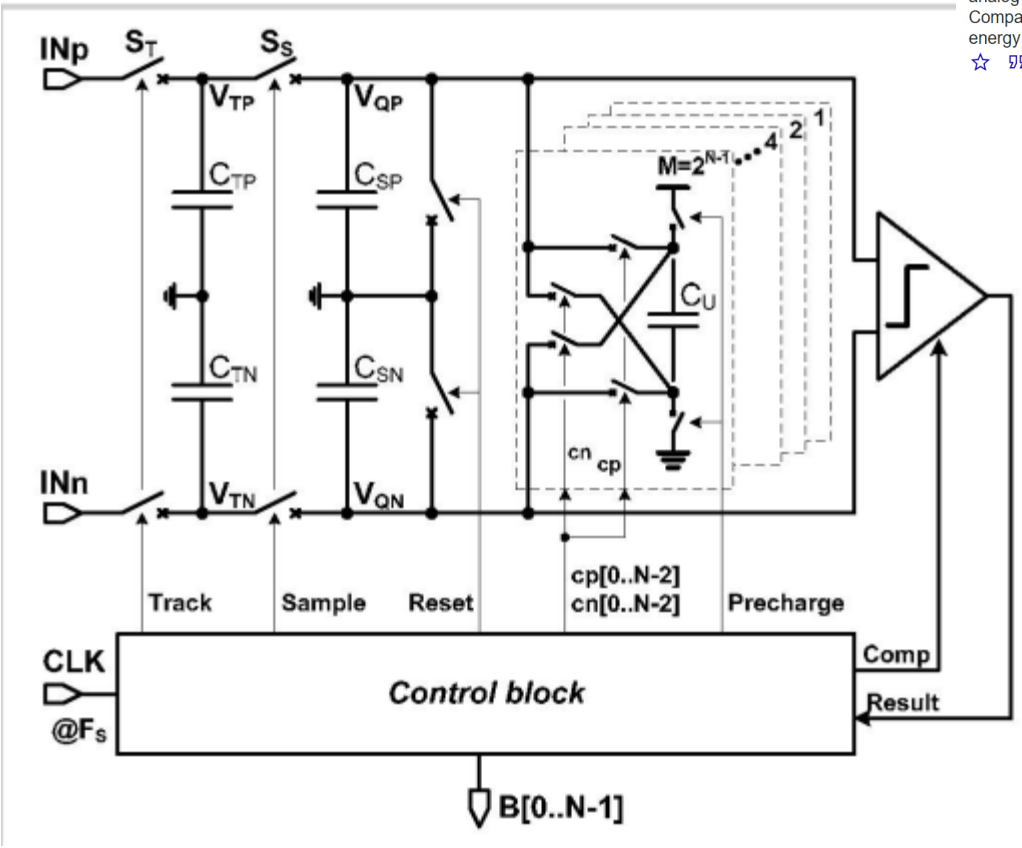
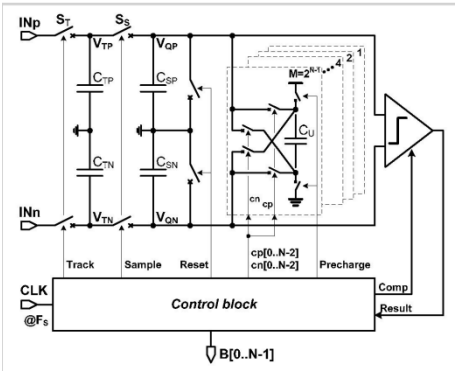


SAR ADC

Charge Sharing ADC with reduced charge redistribution energy

Goal: Have only passive switching



A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7 mW 9b charge-sharing **SAR ADC** in 90nm digital CMOS

J Craninckx, G Van der Plas - Solid-State Circuits Conference, …, 2007 - ieeexplore.ieee.org

Abstract: A fully dynamic **SAR ADC** is proposed that uses passive charge-sharing and an asynchronous controller to achieve low power consumption. No active circuits are needed for high-speed operation and all static power is removed, offering power consumption

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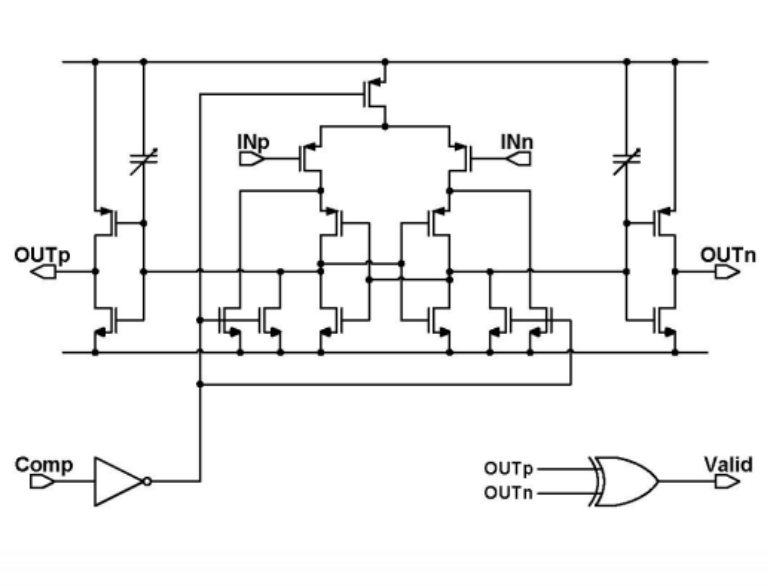

SAR ADC

Lots of ongoing activity in SAR ADCs

A 10-b 600-MS/s 2-way time-interleaved SAR ADC with mean absolu deviation based background timing-skew calibration
Jeonggoo Song ; Nan Sun
2018 IEEE Custom Integrated Circuits Conference (CICC)
Year: 2018
Pages: 1 - 4
Cited by: Papers (2)

A 32 Gb/s ADC-based PAM-4 receiver with 2-bit/stage SAR ADC and partially-unrolled DFE
Shiva Kiran ; Shengchang Cai ; Ying Luo ; Sebastian Hoyos ; Samuel Palermo
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Cited by: Papers (4)

An 11b 80MS/s SAR ADC With Speed-Enhanced SAR Logic and High-Linearity CDAC
Yuefeng Cao ; Yongzhen Chen ; Zhekan Ni ; Fan Ye ; Junyan Ren
2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)
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A 24-to-72GS/s 8b time-interleaved SAR ADC with 2.0-to-3.0pJ/conversion and >30dB SNDR at nyquist in 14nm CMOS FinFET
Lukas Kull ; Danny Luu ; Christian Menolfi ; Matthias Braendli ; Pier Andrea Francese ; Thomas Morf ; Marcel Kossel ; Alessandro Cevrero ; Ilter Ozkaya ; Thomas Toifl
2018 IEEE International Solid - State Circuits Conference - (ISSCC)
Year: 2018
Pages: 358 - 360

A 12-bit 20-MS/s SAR ADC With Fast-Binary-Window DAC Switching in 180nm CMOS
Yung-Hui Chung ; Yi-Shen Lin ; Qi-Feng Zeng
2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)
Year: 2018
Pages: 34 - 37
IEEE Conferences
Abstract (html) (2687 Kb) ©

An 18-bit 2MS/s pipelined SAR ADC utilizing a sampling distortion cancellation circuit with −107dB THD at 100kHz
Derek Hummerston ; Peter Hurrell
2017 Symposium on VLSI Circuits
Year: 2017
Pages: C280 - C281
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A 510nW 12-bit 200kS/s SAR-assisted SAR ADC using a re-switching technique
Yao-Sheng Hu ; Kai-Yue Lin ; Hsin-Shu Chen
2017 Symposium on VLSI Circuits
Year: 2017
Pages: C238 - C239

27.7 A 10b 2.6GS/s time-interleaved SAR ADC with background timing-skew calibration
Chin-Yu Lin ; Yen-Hsin Wei ; Tai-Cheng Lee
2016 IEEE International Solid-State Circuits Conference (ISSCC)
Year: 2016
Pages: 468 - 469
Cited by: Papers (7)

28.4 A 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation
Hai Huang ; Sudipta Sarkar ; Brian Elies ; Yun Chiu
2017 IEEE International Solid-State Circuits Conference (ISSCC)
Year: 2017
Pages: 472 - 473
Cited by: Papers (6)

Background calibration using noisy reference ADC for a 12 b 600 MS/s 2 × TI SAR ADC in 14nm CMOS FinFET
Danny Luu ; Lukas Kull ; Thomas Toifl ; Christian Menolfi ; Matthias Braendli ; Pier Andrea Francese ; Thomas Morf ; Marcel Kossel ; Hazar Yueksel ; Alessandro Cevrero ; Ilter Ozkaya ; Qiuting Huang
ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference
Year: 2017
Pages: 183 - 186

An energy reduced sampling technique applied to a 10b 1MS/s SAR ADC
Harijot Singh Bindra ; Anne-Johan Annema ; Simon M. Louwsma ; Ed J. M. van Tuijl ; Bram Nauta
ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference
Year: 2017
Pages: 235 - 238
Cited by: Papers (2)
IEEE Conferences
Abstract (html) (1347 Kb)

27.3 Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based DAC
Kyojin D. Choo ; John Bell ; Michael P Flynn
2016 IEEE International Solid-State Circuits Conference (ISSCC)
Year: 2016
Pages: 460 - 461
Cited by: Papers (21)
IEEE Conferences
Abstract (html) (662 Kb)

A 0.6 V 12 b 10 MS/s Low-Noise Asynchronous SAR-Assisted Time-Interleaved SAR (SATI-SAR) ADC
Wan Kim ; Hyeok-Ki Hong ; Yi-Ju Roh ; Hyun-Wook Kang ; Sun-Il Hwang ; Dong-Shin Jo ; Dong-Jin Chang ; Min-Jae Seo ; Seung-Tak Ryu
IEEE Journal of Solid-State Circuits
Year: 2016 , Volume: 51 , Issue: 8
Pages: 1826 - 1839
Cited by: Papers (12)

SAR ADC

Lots of ongoing activity in SAR ADCs

Two-step reset method for energy-efficient **SAR ADC** switching schemes [PDF] ieee.org ViewIt@ISU
D Osipov - Electronics Letters, 2016 - IET
… for **SAR ADC**', Electron. Lett., 2013, 49, (5), pp. 327–329 5 Sanyal, A., and Sun, N.: '**SAR ADC** architecture with **98**% reduction in switching energy over conventional scheme', Electron. Lett., 2013, 49, (4), pp. 248–250 6 Zhu, Z …
Cited by 20 Related articles All 2 versions

SAR ADC architecture with **98**% reduction in switching energy over conventional scheme [PDF] ieee.org ViewIt@ISU
A Sanyal, N Sun - Electronics Letters, 2013 - ieeexplore.ieee.org
A high energy-efficiency switching scheme for a successive approximation register (**SAR**) analogue-to-digital converter (**ADC**) is presented. The proposed method can achieve 98.4% savings in switching energy when compared to a conventional **SAR**. The proposed …
Cited by 71 Related articles All 7 versions

Energy-efficient hybrid **capacitor** switching scheme for **SAR ADC** [PDF] ieee.org ViewIt@ISU
L Xie, G Wen, J Liu, Y Wang - Electronics Letters, 2014 - IET
… Introduction: In **successive approximation** register (**SAR**) analogue-to- digital converters (**ADCs**), the digital-to … of DAC **capacitor** arrays [1–5]. The **monotonic** switching technique in [1] achieves an 81.26% reduction in switching energy compared with the conventional **SAR ADC** …
Cited by 51 Related articles All 5 versions

A 0.5 V 1.1 MS/sec 6.3 fJ/conversion-step **SAR-ADC** with tri-level comparator in 40 nm CMOS [PDF] ieee.org ViewIt@ISU
A Shikata, R Sekimoto, T Kuroda… - IEEE Journal of Solid …, 2012 - ieeexplore.ieee.org
This paper presents an extremely low-voltage operation and power efficient successive-approximation-register (**SAR**) analog-to-digital converter (**ADC**). Tri-level comparator is proposed to relax the speed requirement of the comparator and decrease the resolution of …
Cited by 156 Related articles All 11 versions

V_{CM}-based **monotonic capacitor** switching scheme for **SAR ADC** [PDF] ieee.org ViewIt@ISU
Z Zhu, Y Xiao, X Song - Electronics Letters, 2013 - ieeexplore.ieee.org
A novel energy-efficient V CM-based **monotonic capacitor** switching scheme for **successive approximation** register (**SAR**) analogue to-digital converters (**ADCs**) is proposed. Based on the third reference voltage V CM and **monotonic capacitor** switching procedure, the …
Cited by 93 Related articles All 4 versions

[PDF] **A 10-bit** 50-MS/s **SAR ADC** with **a monotonic capacitor** switching procedure [PDF] ncku.edu.tw ViewIt@ISU
CC Liu, SJ Chang, GY Huang… - IEEE Journal of Solid …, 2010 - msicdt.ee.ncku.edu.tw
This paper presents **a** low-power **10-bit** 50-MS/s suc-cessive approximation register (**SAR**) analog-to-digital converter (**ADC**) that uses **a monotonic capacitor** switching procedure. Compared to converters that use **the** conventional procedure, **the** average switching energy …
Cited by 788 Related articles All 10 versions

22.1 A 90GS/s 8b 667mW 64× interleaved **SAR ADC** in 32nm digital SOI CMOS [PDF] ieee.org ViewIt@ISU
L Kull, T Toifl, M Schmatz, PA Francese… - … Solid-State Circuits …, 2014 - ieeexplore.ieee.org
Forthcoming optical communication standards such as ITU OTU-4 and 100/400Gb/s Ethernet require ADCs with more than 50GS/s and at least 5 ENOB to enable complex equalization in the digital domain. **SAR** ADCs and interleaved ADCs made impressive …
Cited by 139 Related articles All 7 versions

SAR ADC

Lots of ongoing activity in SAR ADCs

An ultra low energy 12-bit rate-resolution scalable **SAR ADC** for wireless sensor nodes
N Verma, AP Chandrakasan - IEEE Journal of Solid-State …, 2007 - ieeexplore.ieee.org
Abstract: A resolution-rate scalable **ADC** for micro-sensor networks is described. Based on the successive approximation register (**SAR**) architecture, this **ADC** has two resolution modes: 12 bit and 8 bit, and its sampling rate is scalable, at a constant figure-of-merit, from 0-
Cited by 312 Related articles All 16 versions Cite Save More

A 10-bit 100-MS/s reference-free **SAR ADC** in 90 nm CMOS
Y Zhu, CH Chan, UF Chio, SW Sin… - IEEE Journal of Solid …, 2010 - ieeexplore.ieee.org
Abstract: A 1.2 V 10-bit 100 MS/s Successive Approximation (SA) **ADC** is presented. The scheme achieves high-speed and low-power operation thanks to the reference-free technique that avoids the static power dissipation of an on-chip reference generator.
Cited by 323 Related articles All 16 versions Cite Save More

Merged capacitor switching based **SAR ADC** with highest switching energy-efficiency
V Hariprasath, J Guerber, SH Lee… - Electronics Letters, 2010 - ieeexplore.ieee.org
Abstract: A modified merged capacitor switching (MCS) scheme is proposed for the successive approximation register (**SAR**) analogue-to-digital converter (**ADC**). The conventional MCS technique previously applied to a pipelined **ADC** improves signal
Cited by 160 Related articles All 10 versions Cite Save More

SAR ADC

Lots of ongoing activity in SAR ADCs

An 820μW 9b 40MS/s noise-tolerant dynamic-**SAR ADC** in 90nm digital CMOS

V Giannini, P Nuzzo, V Chironi… - Solid-State Circuits …, 2008 - ieeexplore.ieee.org

Abstract: Current trends in analog/mixed-signal design for battery-powered devices demand the adoption of cheap and power-efficient ADCs. **SAR** architectures have been recently demonstrated as able to achieve high power efficiency in the moderate-resolution/medium-

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A 10b 100MS/s 1.13 mW **SAR ADC** with binary-scaled error compensatior

CC Liu, SJ Chang, GY Huang, YZ Lin… - Solid-State Circuits …, 2010 - ieeexplore.ieee.org

Abstract: In recent years, due to the improvements in CMOS technologies, medium resolution (8 to 10b) **SAR** ADCs have been able to achieve sampling rates of several tens of MS/s with excellent power efficiency and small area [1]–[4]. When the sampling rate

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A 9.4-ENOB 1V 3.8 μW 100kS/s **SAR ADC** with time-domain comparator

A Agnes, E Bonizzoni, P Malcovati… - Solid-State Circuits …, 2008 - ieeexplore.ieee.org

Abstract: The **ADC-SAR** is fabricated in a 0.18 mum 2P5M CMOS process. This **SAR-ADC** converter achieves 56fJ/conversion-step FOM with 58dB SNDR. It uses a comparator, named time-domain comparator, that instead of operating in the voltage domain, transforms

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SAR ADC

Lots of ongoing activity in SAR ADCs

A 12b 22.5/45MS/s 3.0 mW 0.059 mm 2 CMOS **SAR ADC** achieving over 90dB SFDR

W Liu, P Huang, Y Chiu - Solid-State Circuits Conference …, 2010 - ieeexplore.ieee.org

Abstract: CMOS technology scaling has opened a pathway to high-performance analog-to-digital conversion in the nanometer regime, where switching is preferred over amplifying. Successive-approximation-register (**SAR**) is one of the conversion architectures that rely on

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A 1.1 v 50mw 2.5 gs/s 7b time-interleaved c-2c **sar adc** in 45 cmos

E Alpman, H Lakdawala, LR Carley… - Solid-State Circuits …, 2009 - ieeexplore

Abstract: High-speed medium-resolution ADCs are widely utilized in high-speed communication systems, such as serial links, UWB, and OFDM-based 60 GHz r Due to complex DSP and low-power constraints, digital basebands are designec

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A 1.1 v 50mw 2.5 gs/s 7b time-interleaved c-2c **sar adc** in 45nm lp digital cmos

E Alpman, H Lakdawala, LR Carley… - Solid-State Circuits …, 2009 - ieeexplore.ieee.org

Abstract: High-speed medium-resolution ADCs are widely utilized in high-speed communication systems, such as serial links, UWB, and OFDM-based 60 GHz receivers. Due to complex DSP and low-power constraints, digital basebands are designed in low-

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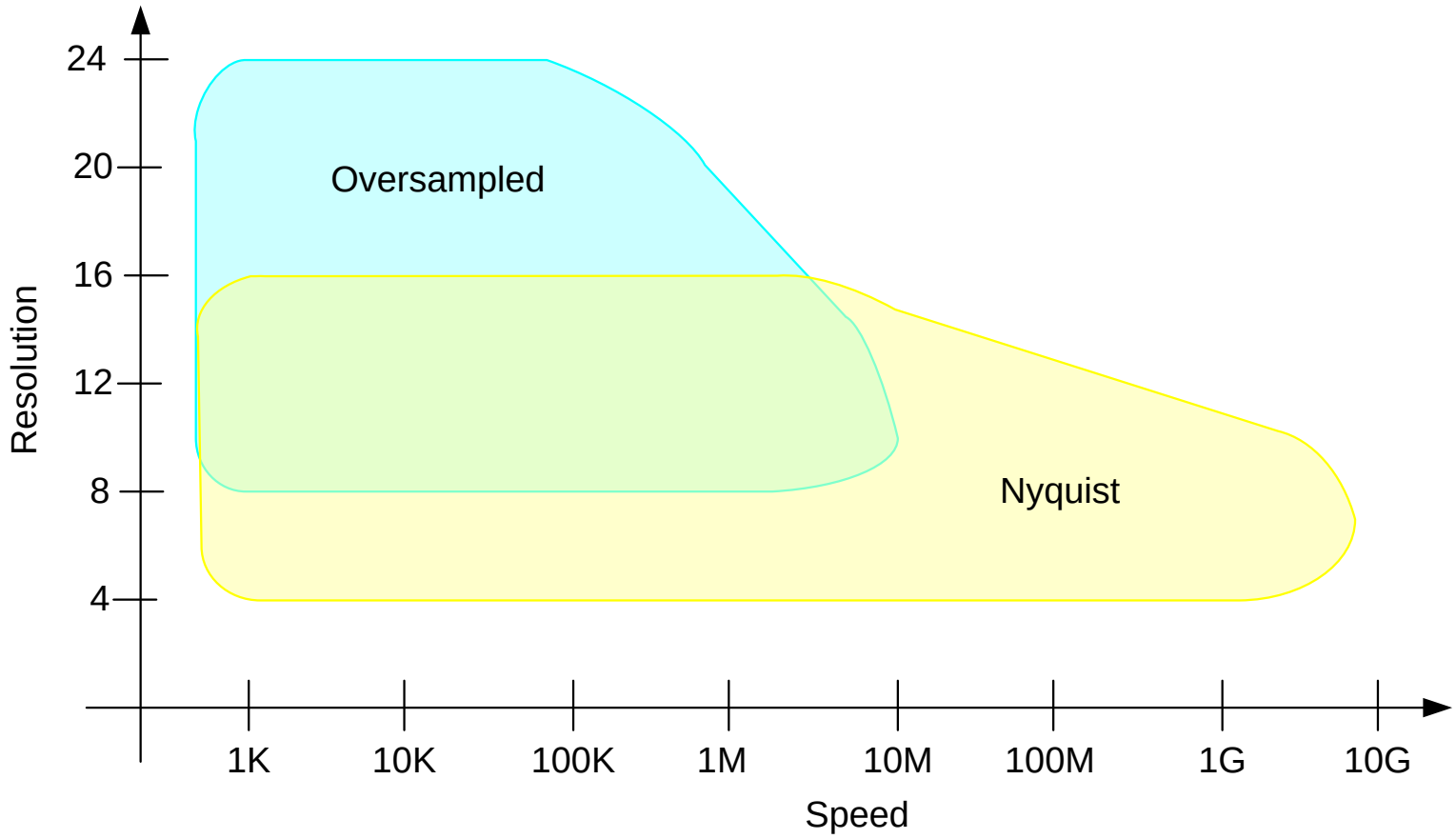
Data Converter Type Chart



Stay Safe and Stay Healthy !

End of Lecture 27